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MS-7B24 mATX Ver: 1.020

PC MATE BAZOOKA

Coffeelake Platform

CPU: Coffeelake S

PCH H370B360

SPI ROM: 128MB

Memory: DDR4* 4(Dual Channel)

Power Solution

CPU: RI3607

VCCSA: RI8125E

VCCIO: SY8288

DDR: RI8125E

PCH: RI8125E

ACPE MPS

Onboard Chip

LAN RIL8111H

Dual Codec: ALC887

SIO NCIG797/6795D

Type C: ASM1543

USB3 Redrive: NB7VPQ702X1

GPIO: NCI5605* 2

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

M2 Slot (Socket 1) * 1

LED

EZ Debug LED

Audio Line LED

BOT LED

Rear I/O Connectors

PS2

USB2.0x2

USB3.1 Gen1x2

RJ45+ USB3.1 (Type C+ A)

Audio Jack 3Port

HDMI+ (DVI/DVI+VGA)

Internal Connectors

Dual SATA * 1

SINGLE SATA * 4

FUSE30 Header* 1

FUSE20 Header* 2

Front Audio Header* 1

Front Panel Header* 2

SPI Header* 1

TPM Header* 1

CPU Fan * 1

System Fan * 2

Internal Pin Header

JRGB1

JSPI1

JIBT1

JBAT1

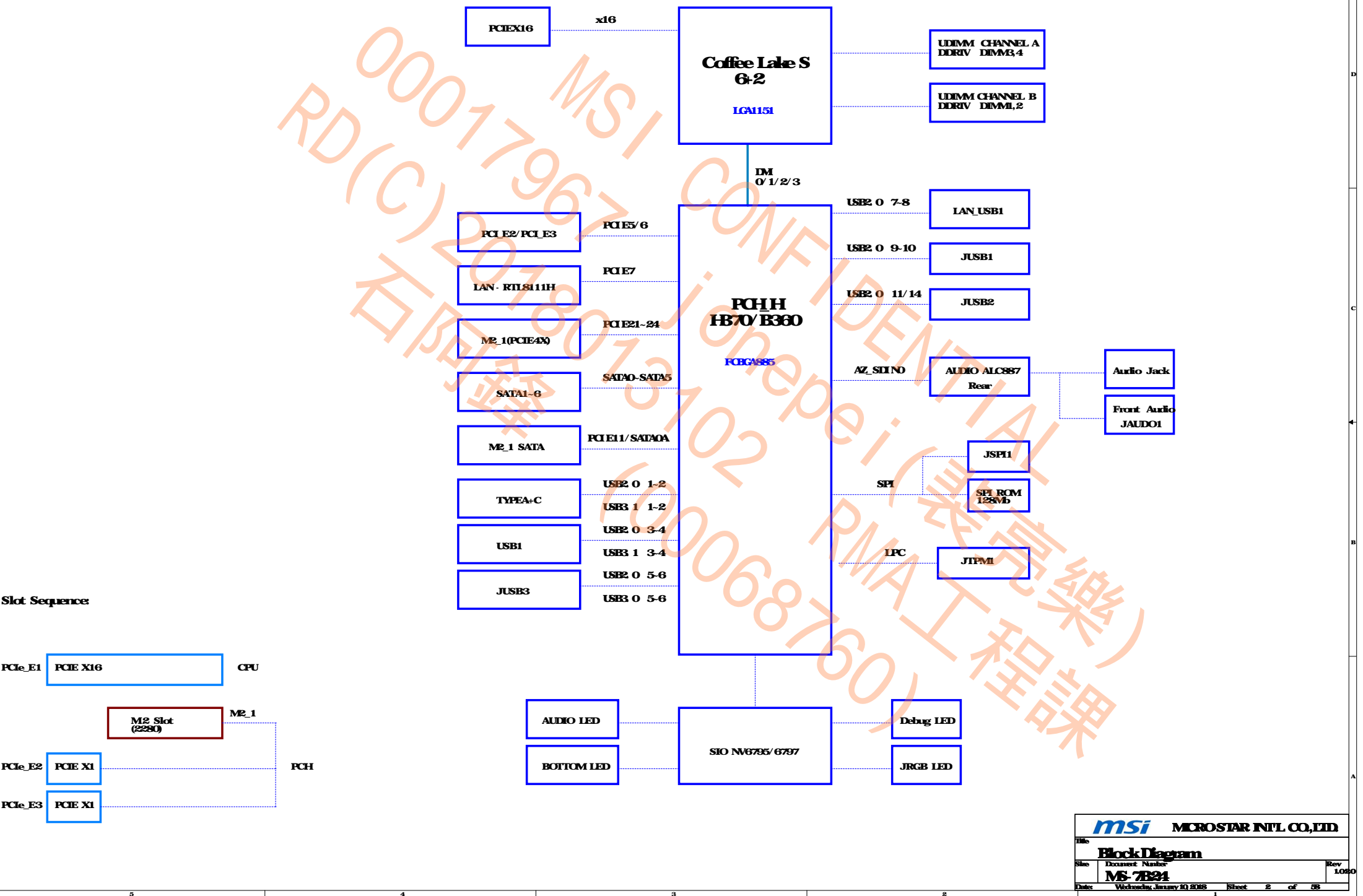
JCI1

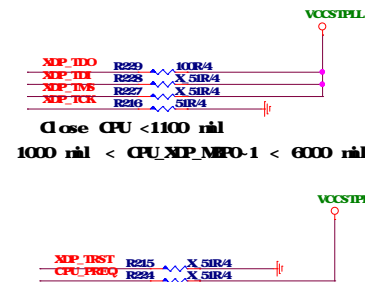
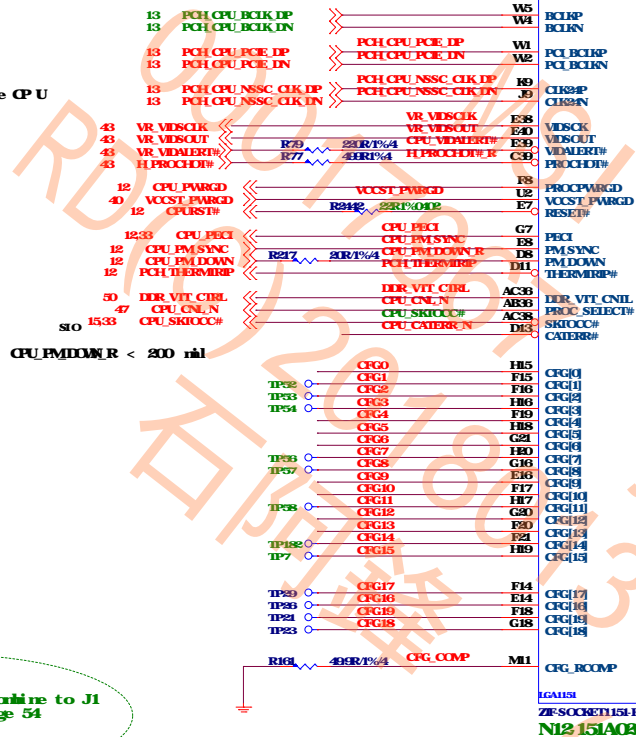
JTPM1

JCOM1

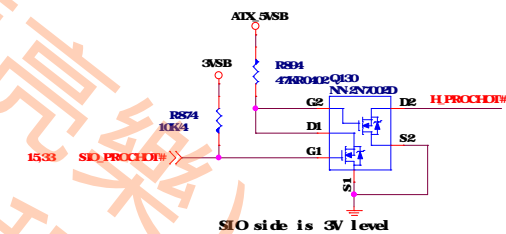
JLPT1

MS-7B24 Block Diagram

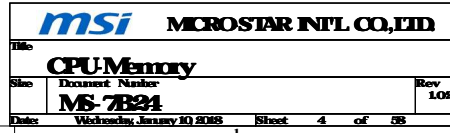


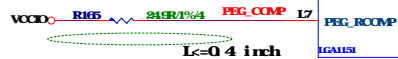
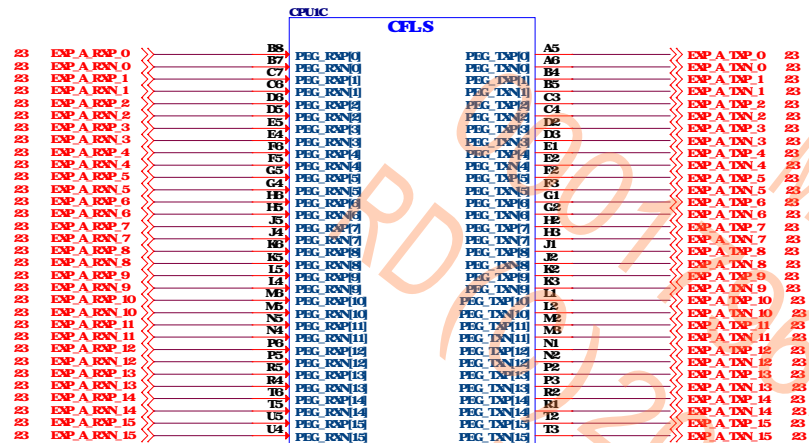


ZF-SOCKET151-HF
N12 151A020 F02

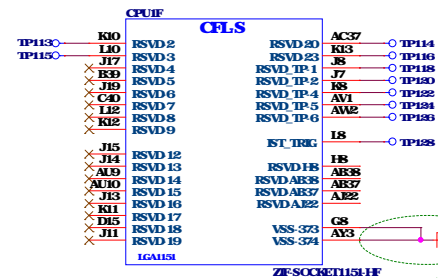


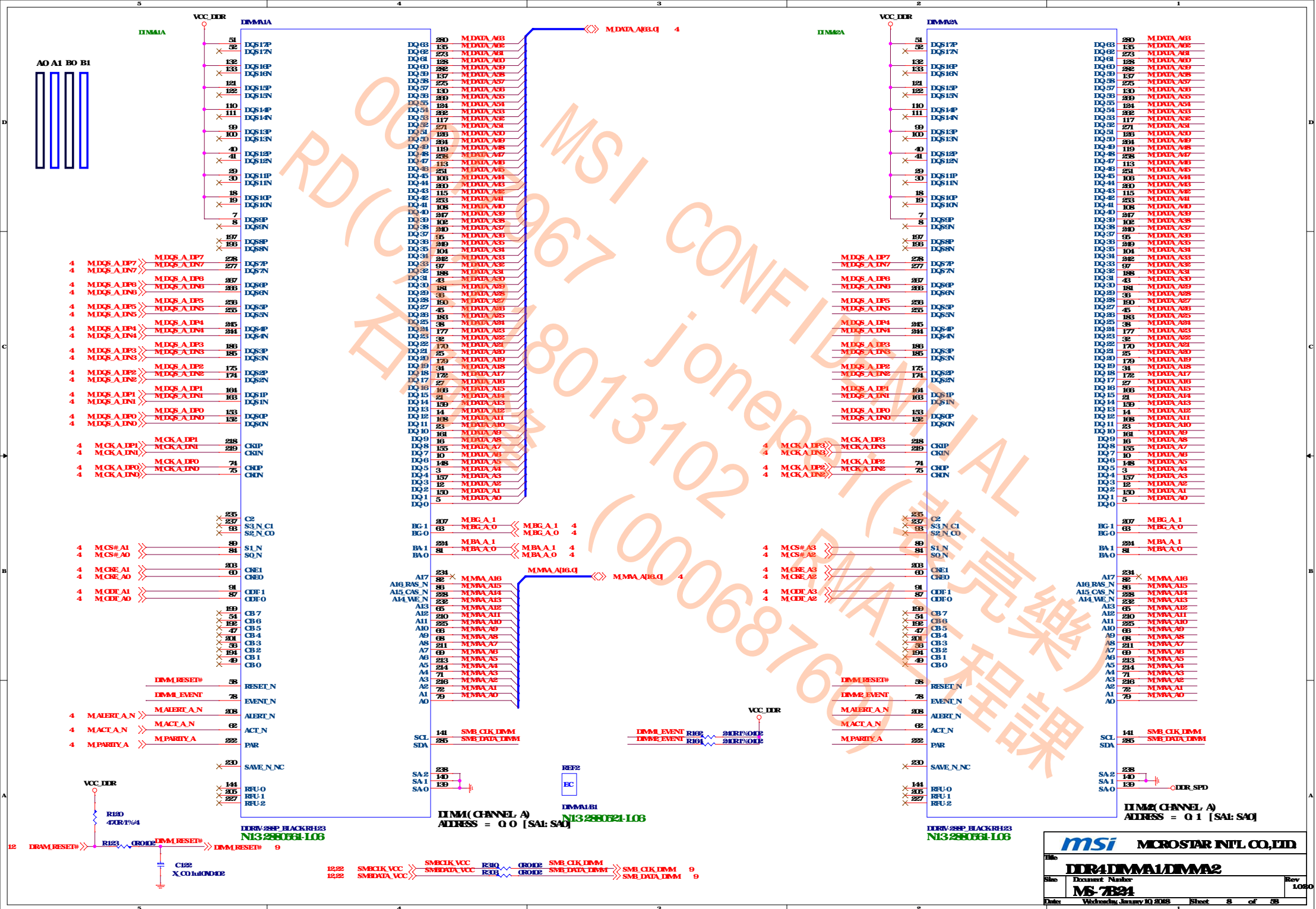
CRC Table			
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	FCU PLL Lock
2	NORM	REVERSE	PEG, LANE, REVERSE, RSD
3			
4	DISABLE	ENABLE	eEP
5	DISABLE	ENABLE	PEGLOCKB [1]
6	DISABLE	ENABLE	PEGLOCKB [0]
7	RESET#	BUS REQ	PEG, DEEPER, TBM/UNING
8			
9	PRESENT	NO PRESENT	SAME PRESENT
10			RSD
11			RSD
12			RSD
13			RSD
14			RSD
15			RSD
16			RSD
17			RSD
18			RSD
19			RSD

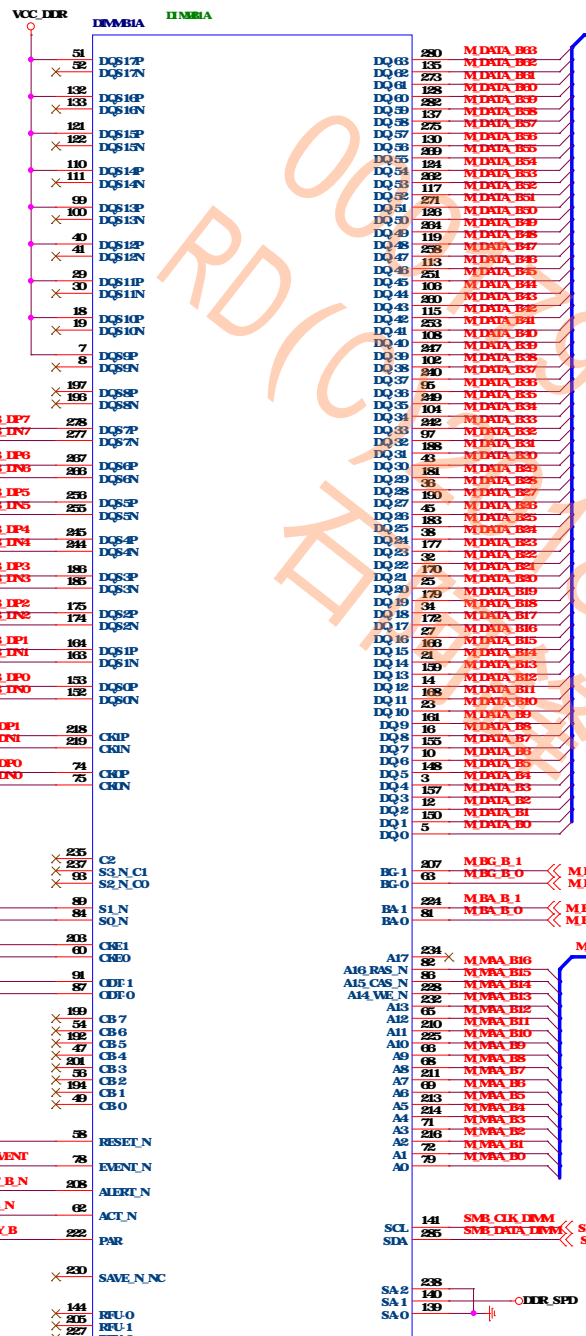




IGA1151
ZF-SOCKET1151.HF
N12 151A080F02

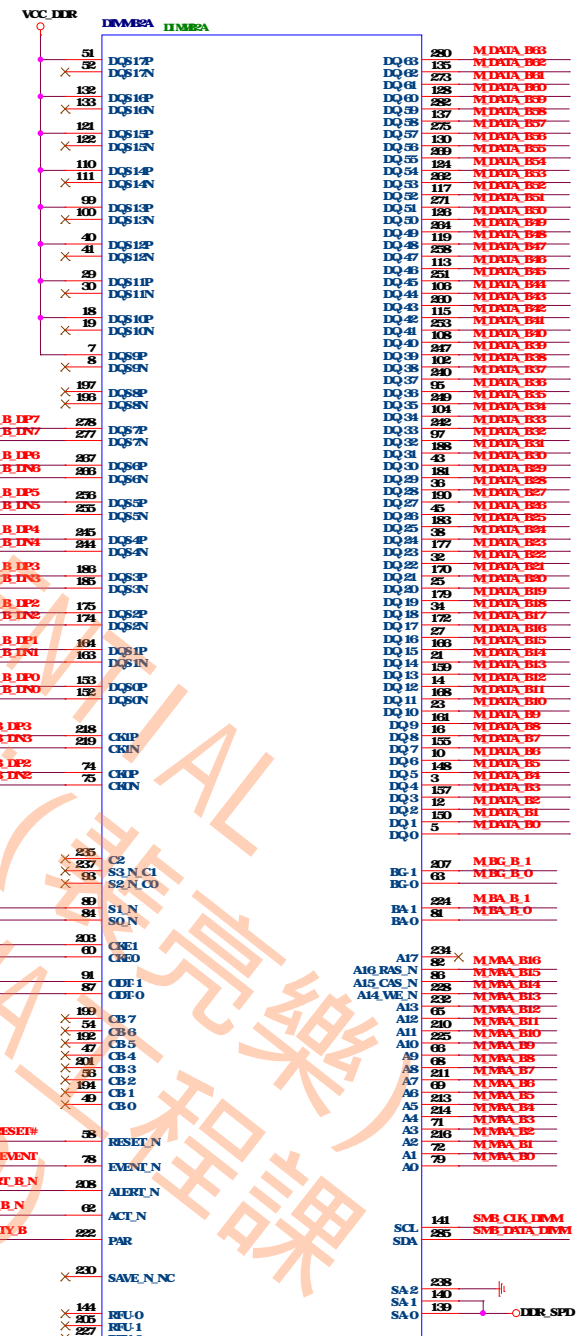






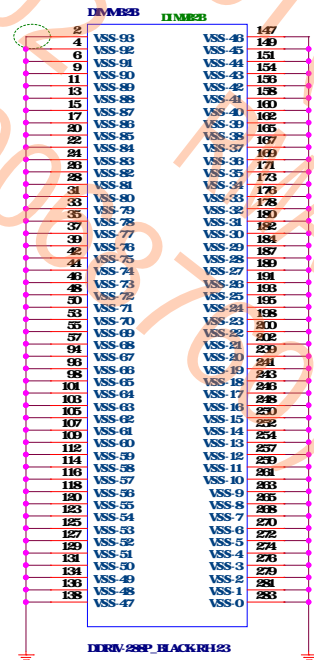
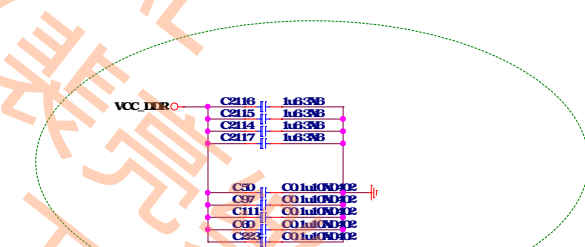
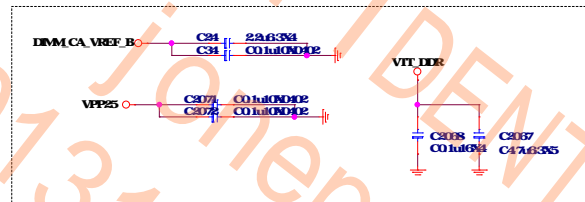
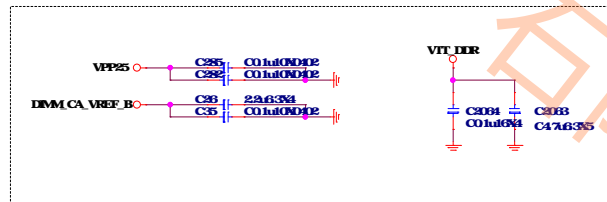
DDR4-288P, BLACKH423
N132880661-106

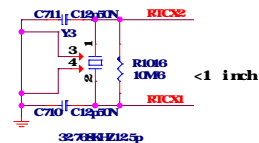
DIMM1 (CHANNEL B)
ADDRESS = 1:0 [SA1:SA0]



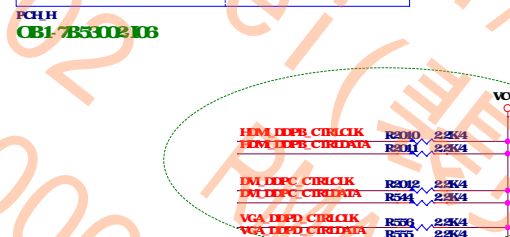
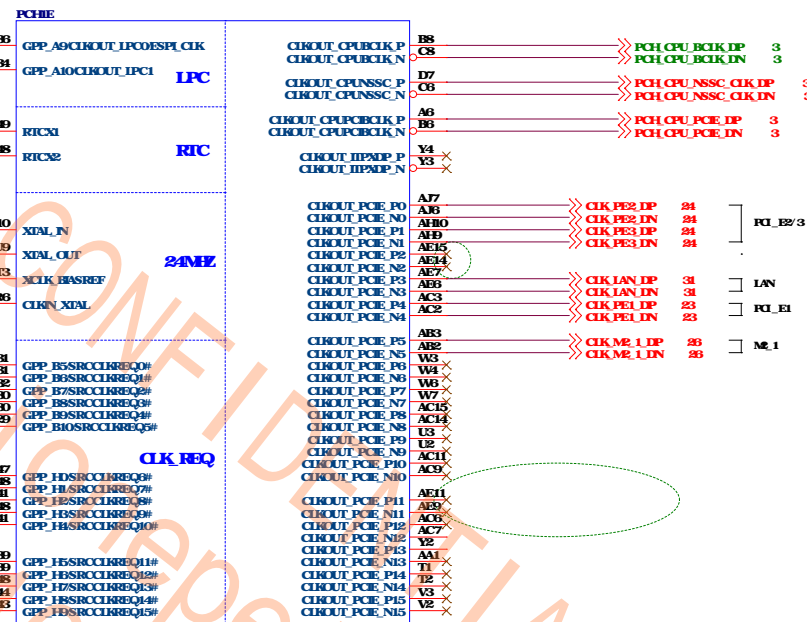
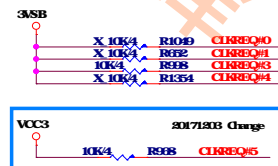
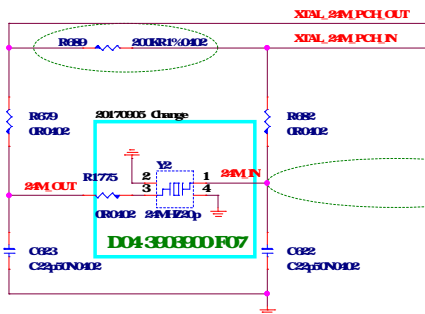
DDR4-288P, BLACKH423
N132880661-106

DIMM2 (CHANNEL B)
ADDRESS = 1:1 [SA1:SA0]





2017/7/11
The value of R689 is the same as FIG r0.9 by Intel's feedback

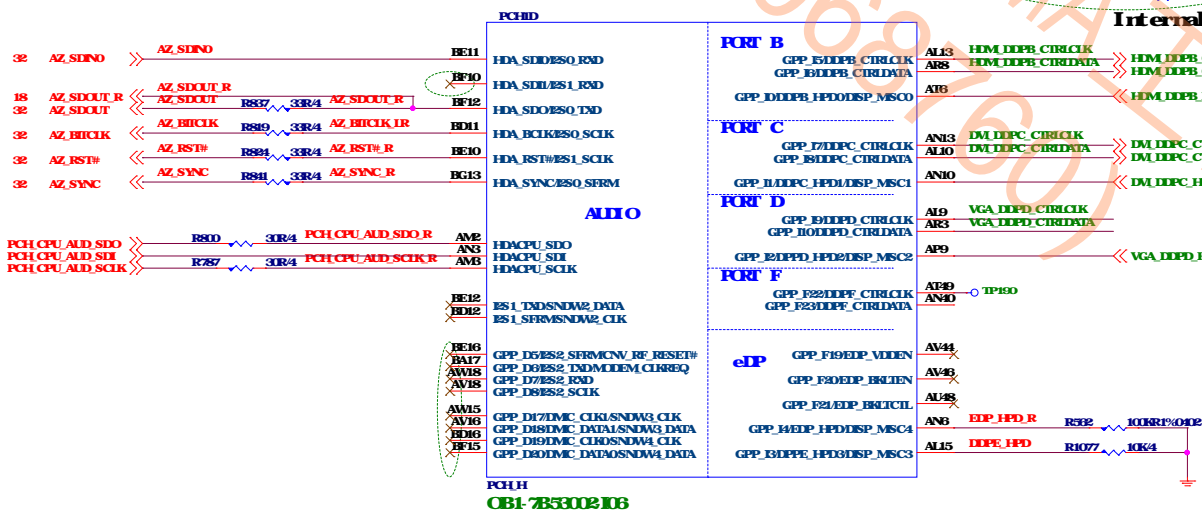


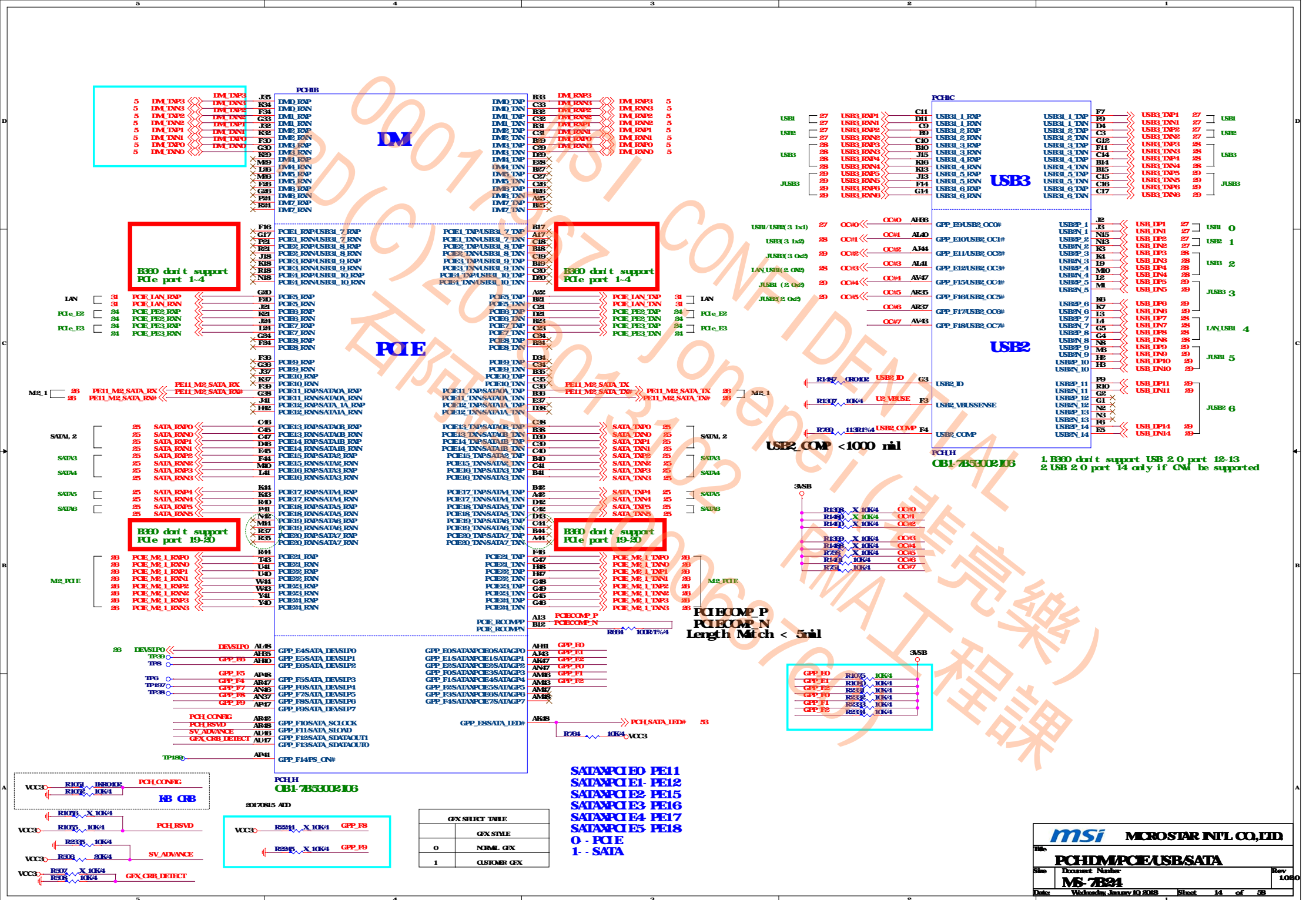
Internal pull-down is disabled after PCH_PMRK is high

0 : Port B is not detected (Default)
1 : Port B is detected

0: Port C is not detected (Default)
1: Port C is detected

0 : Port D is not detected (Default)
1 : Port D is detected

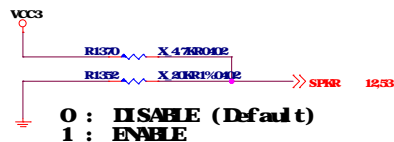




VSS

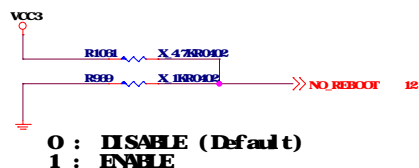
OB1-7B53002106

TOP Swap



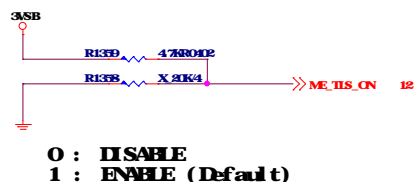
Internal pull-down is disabled after PCH_PWCK is high

No Reboot



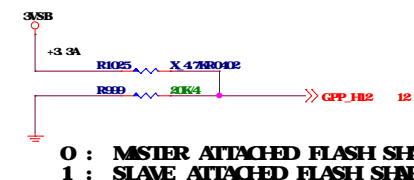
Internal pull-down is disabled after PCH_PWCK is high

TLS confidentiality



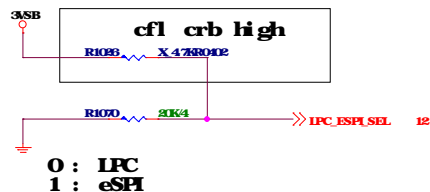
Internal pull-down is disabled after RSMST# de-assert.

ESPI FLASH SHARING MODE



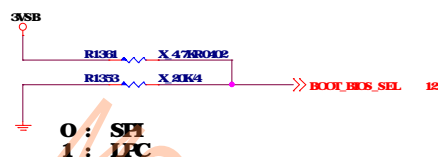
Internal pull-down is disabled after RSMST# de-assert.

LPC eSPI Mode



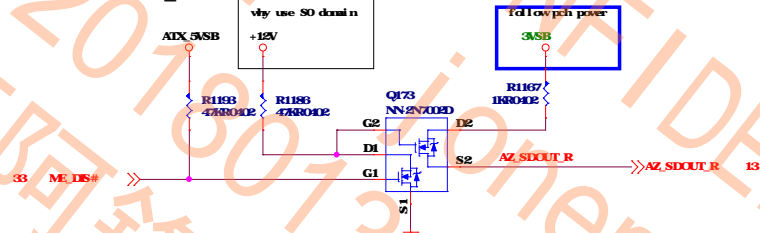
Internal pull-down is disabled after RSMST# de-assert.

Boot HCS



Internal pull-down is disabled after PCH_PWCK is high

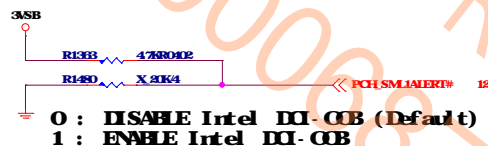
HDA_SDO



0 : Enable security measures defined in the Flash Descriptor.
(Default)
1 : DISABLE Flash Descriptor Security(Override).

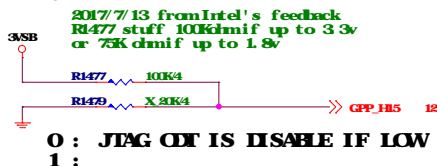
Internal pull-down is disabled after PCH_PWCK is high

DI ENABLE

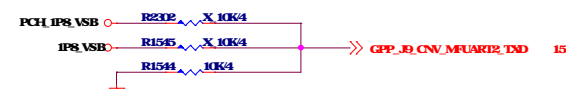


Internal pull-down is disabled after RSMST# de-assert.

ODT DISABLE



SELECT THE SPI HCS FLASH INTERFACE OPERATING VOLTAGE



0 = VCCSPI IS CONNECTED TO 3.3V RAIL (DEFAULT)
1 = VCCSPI IS CONNECTED TO 1.8V RAIL
PCH HAS INTERNAL 20K PD

201704 CHINE

XIAL FREQUENCY SELECTION

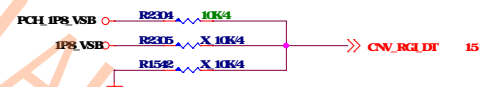


1 = 24MHZ (25MHZ WHEN XIAL_FREQ_DIVIDER NON ZERO)
0 = 38.4/19.2MHZ

XIAL_SEL1 : Internal Pull down

MODEM AND NFC REFERENCE CLOCK SOURCE SELECT

2017/7/12 from Intel's feedback
FU if the integrated CNM is enabled
PD if the integrated CNM is disabled



CNM_BS
0 = Integrated CNM enable
1 = Integrated CNM disable

20170816 change

XIAL INPUT MODE



1 = XIAL INPUT IS DIFFERENTIAL
0 = XIAL INPUT IS SINGLE ENDED
PCH HAS INTERNAL 20K PD

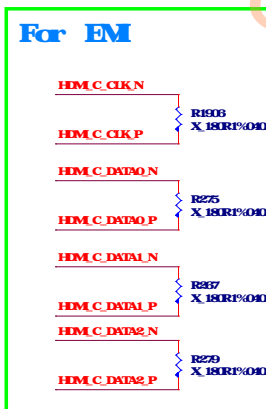
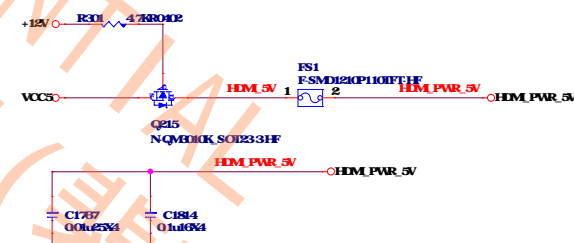
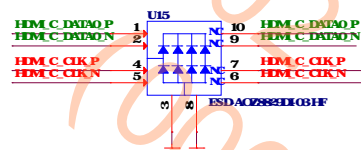
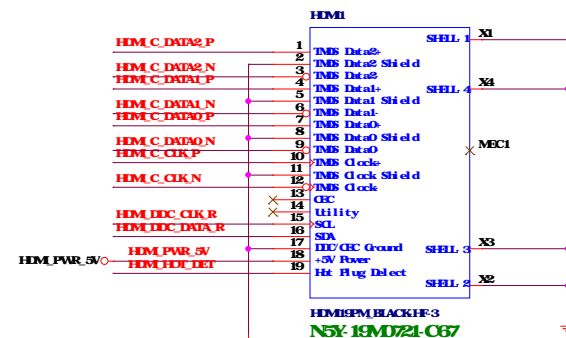
msi MICROSTAR INT'L CO., LTD.

Title	PCHStrap	Rev	1.00
Doc Number	MS-7B24	Rev	1.00
Date	Wednesday, January 10, 2018	Sheet	15 of 58

For EM

HIM.C.CLK.N
HIM.C.CLK.P
HIM.C.DAT0.N
HIM.C.DAT0.P
HIM.C.DAT1.N
HIM.C.DAT1.P
HIM.C.DAT2.N
HIM.C.DAT2.P
HIM.C.DAT3.N
HIM.C.DAT3.P

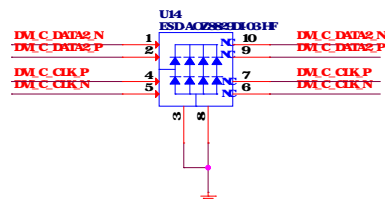
R1809
X 180R0102
R275
X 180R0102



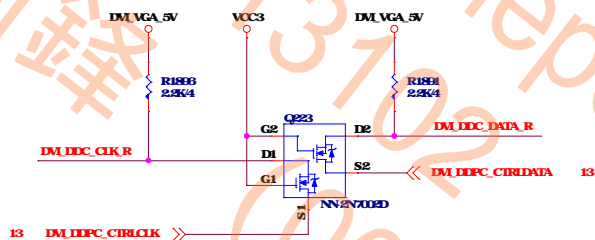
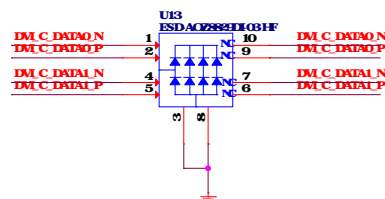
VGA resolution of 2048x1536 pixels with 32 bit color at 75 Hz (4:3 QGA)



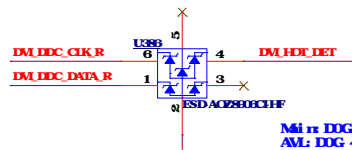
U14 AM: IDG 05A050C Q15
IDG 06A050C A68



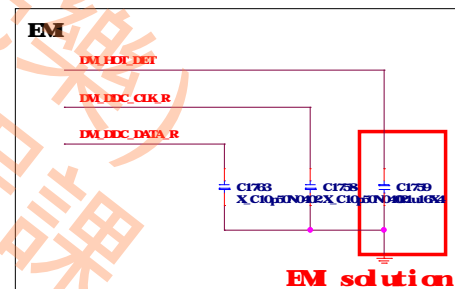
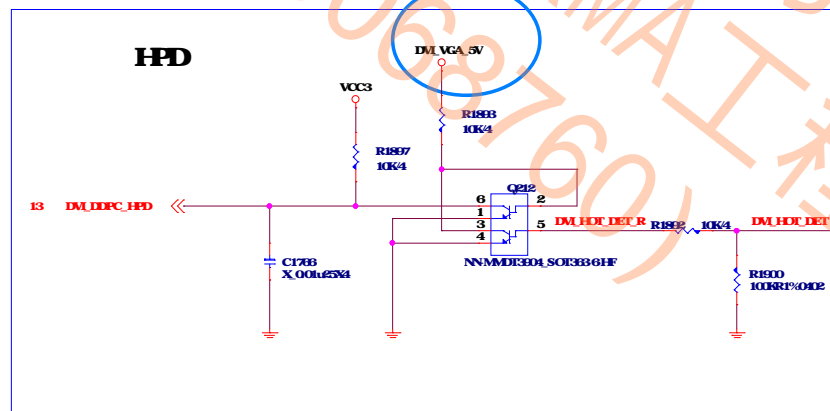
U17 AM: IDG 05A050C Q15
IDG 06A050C A68



EMI Gap near connector DM1



Mit IDG 05A050C A68
Mit IDG 45B0510 114

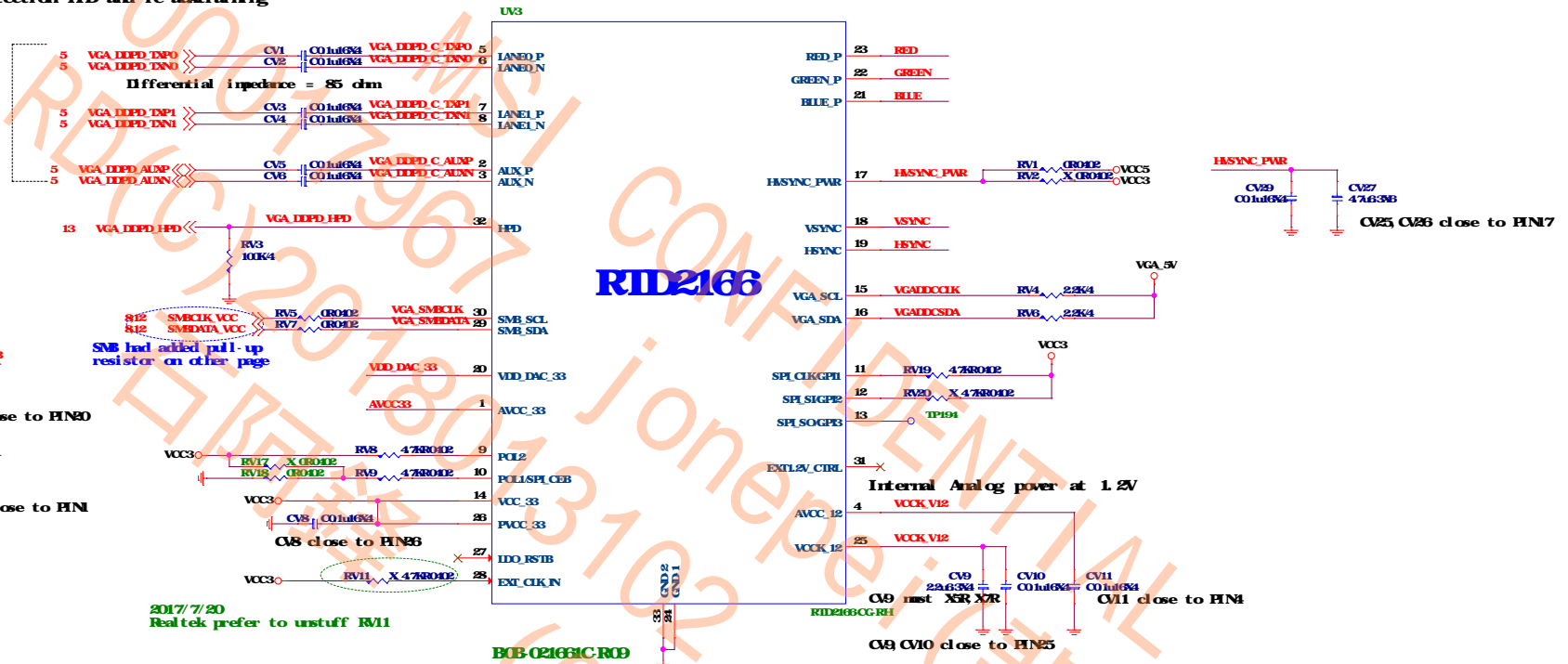


msi MICROSTAR INT'L CO., LTD.

Doc# MS-7B24
Rev 1.00
Date: Wednesday, January 11, 2006 Sheet 21 of 28

Note:

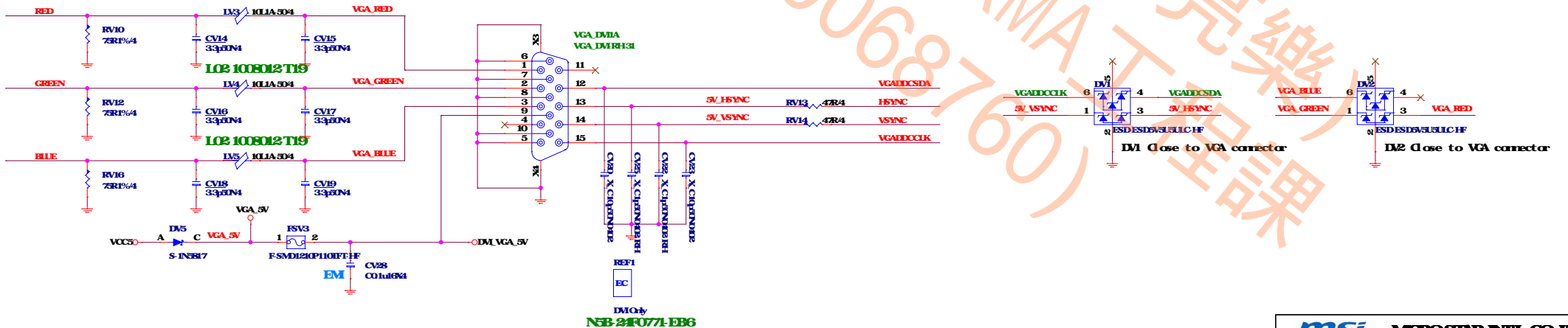
If connect to eDP port, must confirm whether it support hot plug detection HPD and re-auditing



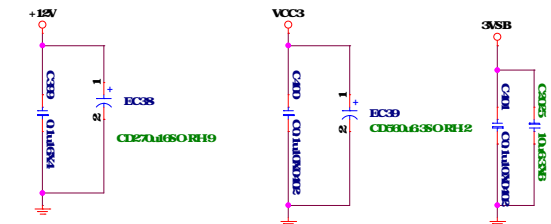
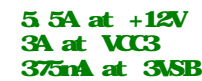
L02 1008012 T19

L02 1008012 T19

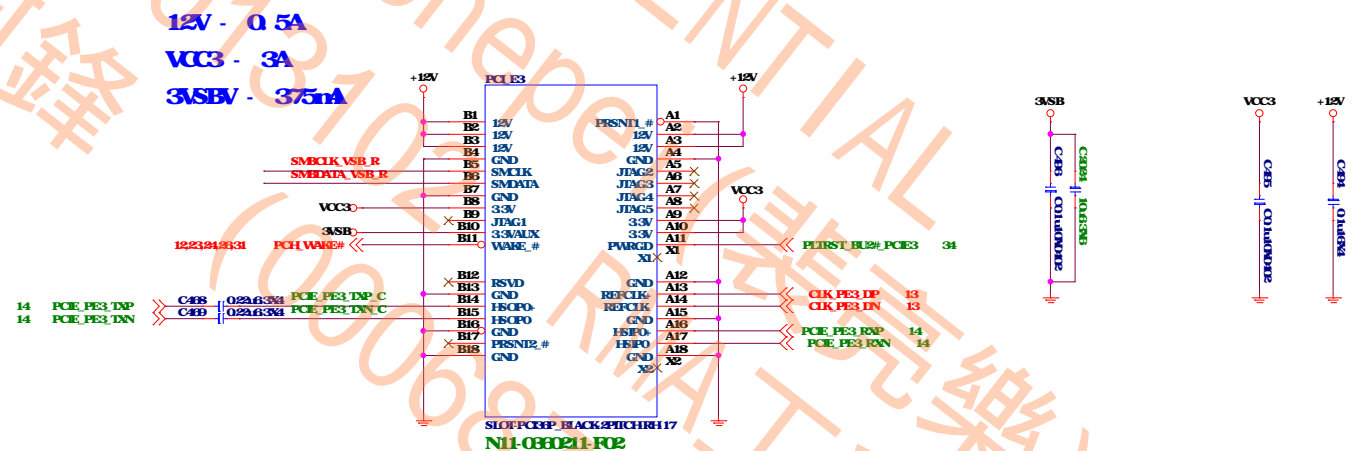
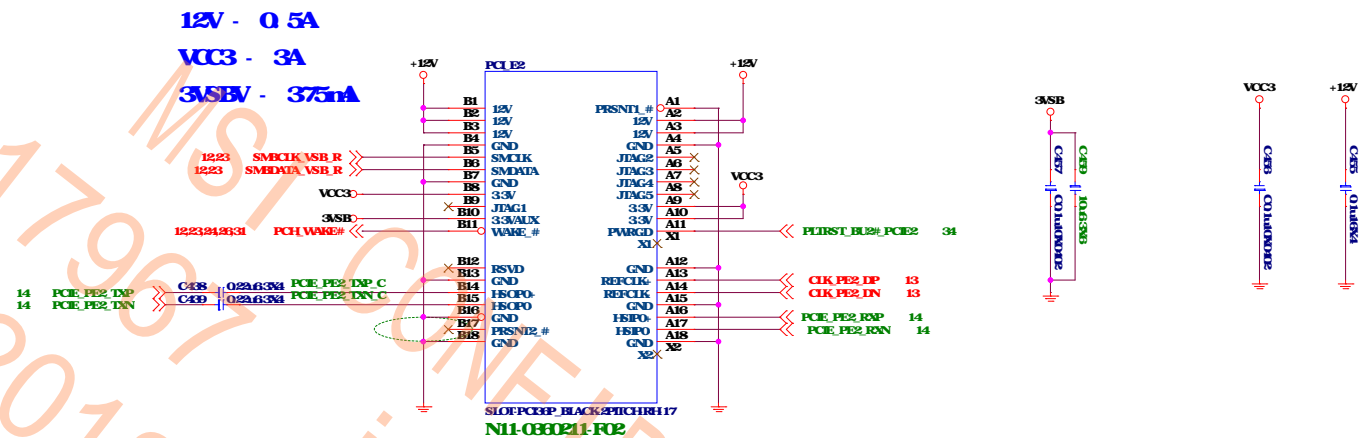
L02 1008012 T19

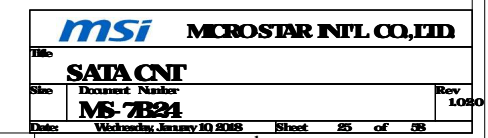


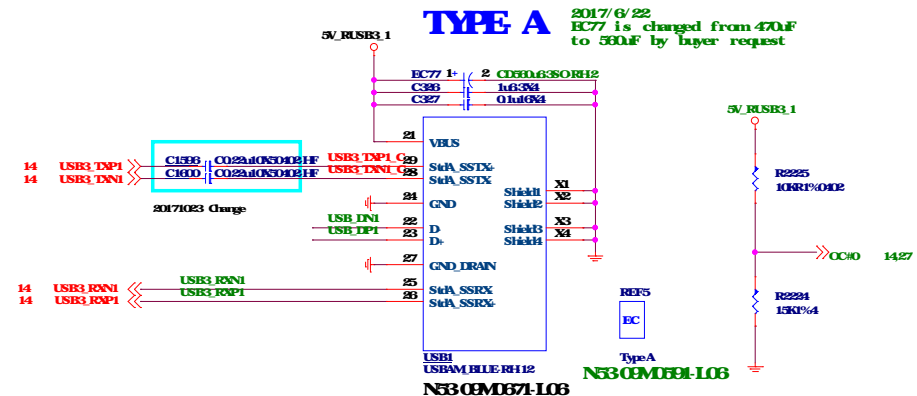
N3B 2F0771-EB6



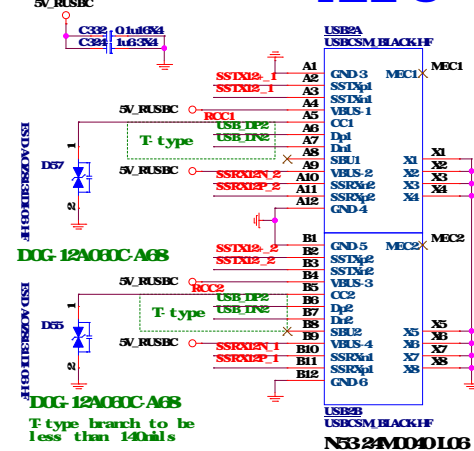
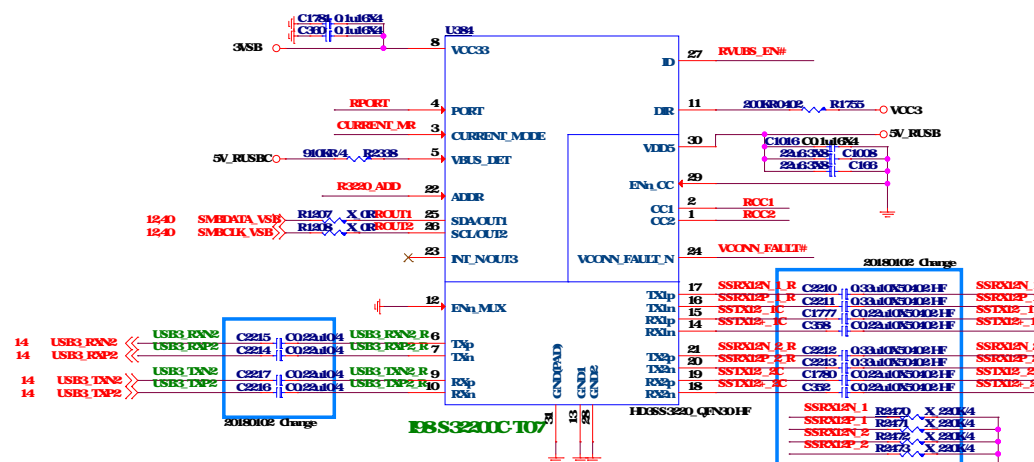
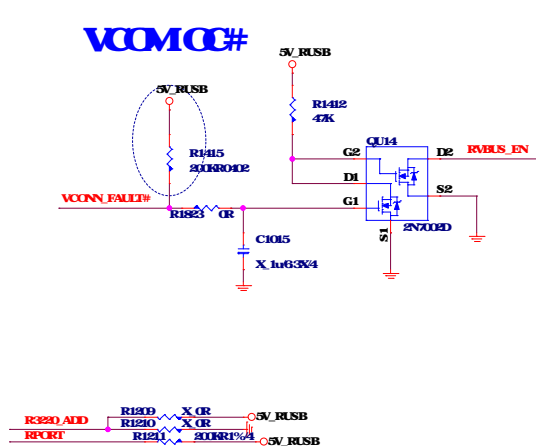
PCH PCIe X1 Slot



[illegible]

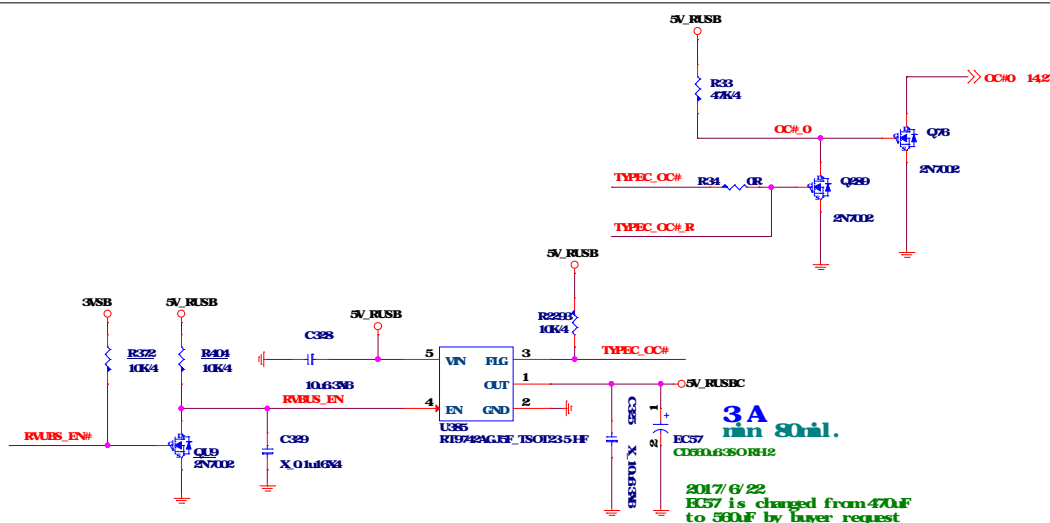
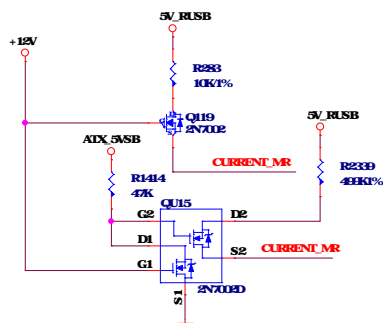


close to Connector USB5 **TYPE C**

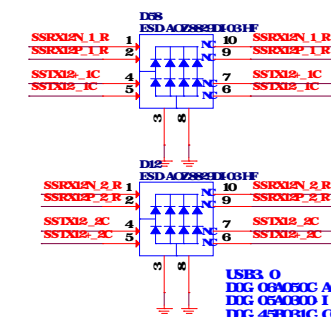


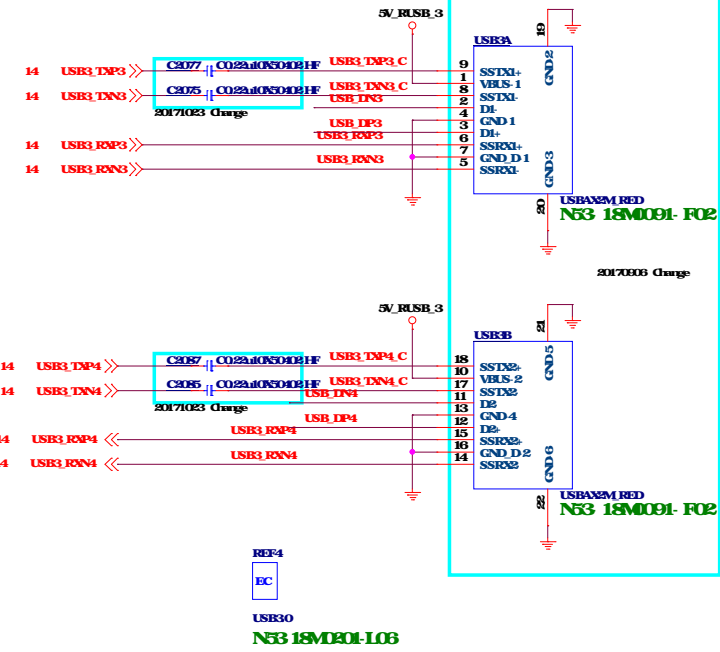
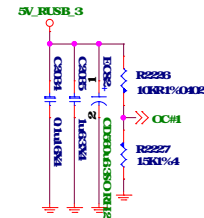
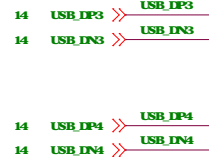
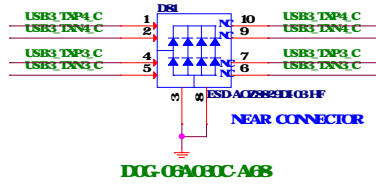
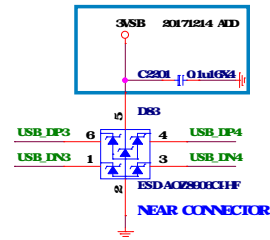
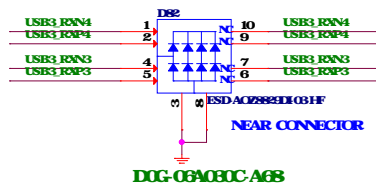
Current Mode

L - Default for 900mA
M- Mid (500K) for 1.5A
H- High (10K) for 3A

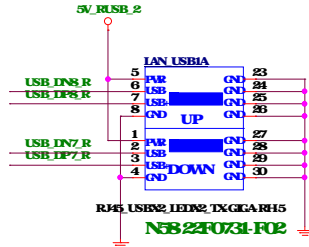
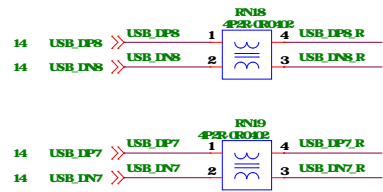


ESD Protection
NEAR CONNECTOR

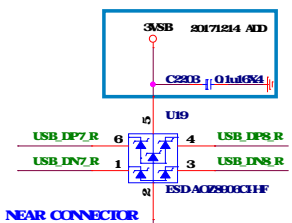
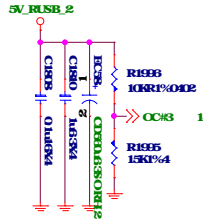




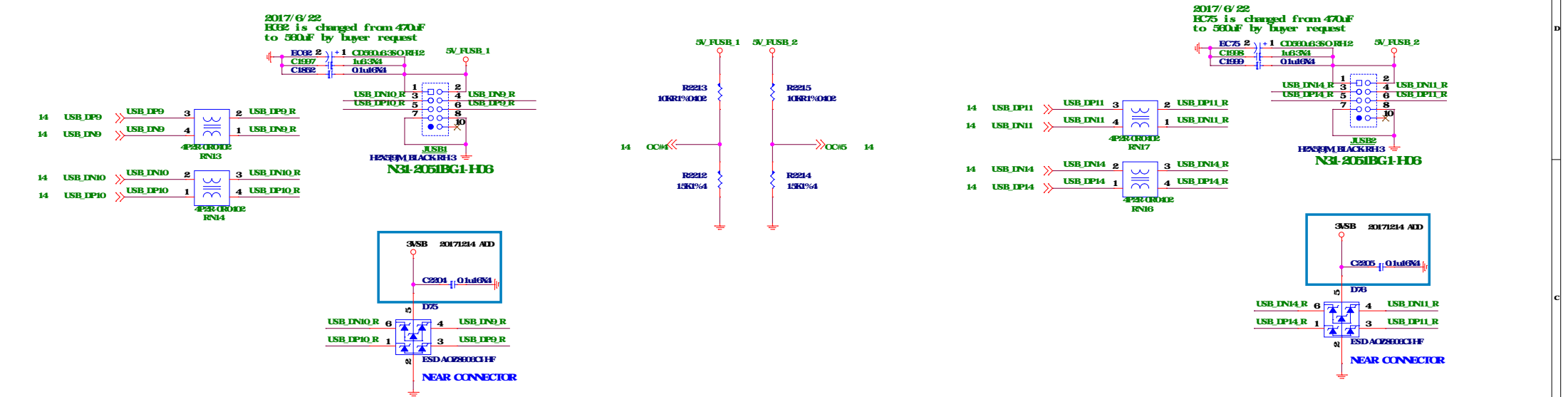
LAN_USB1



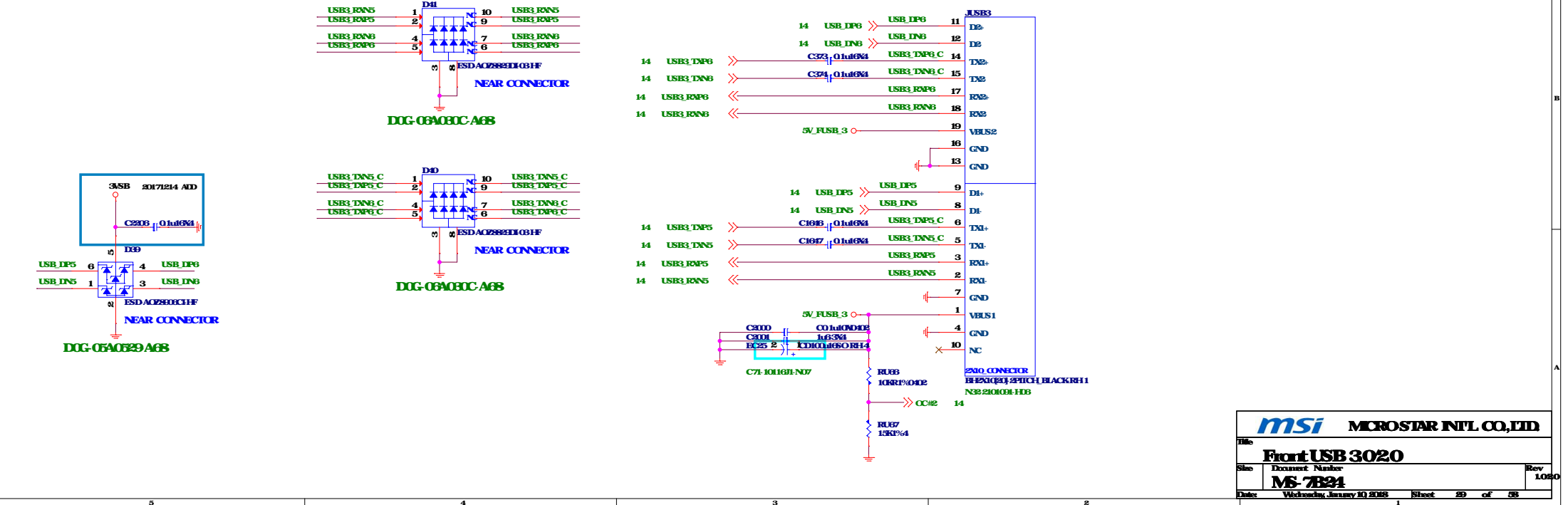
2017/6/22
EC58 is changed from 470uF
to 560uF by buyer request



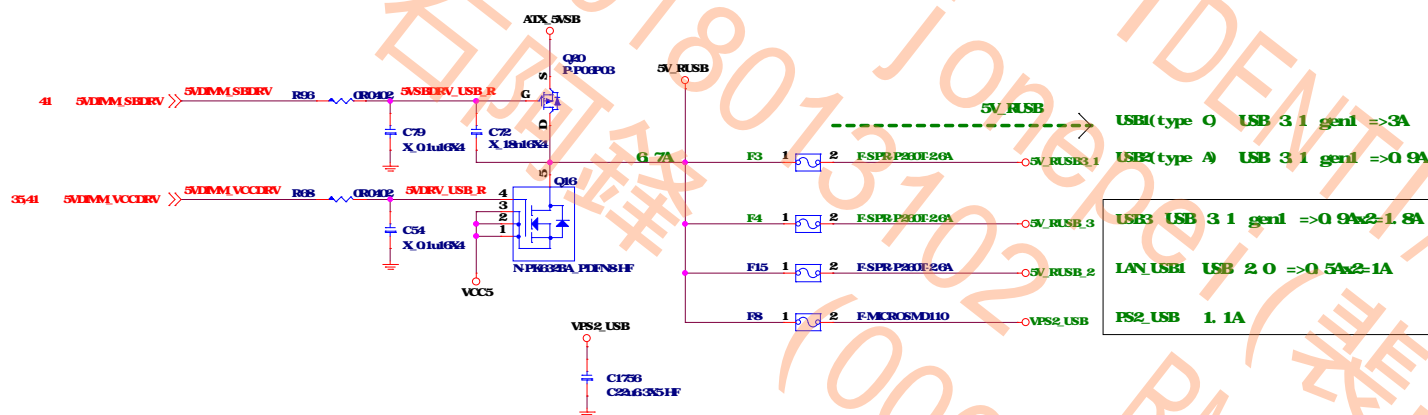
FRONT USB2.0



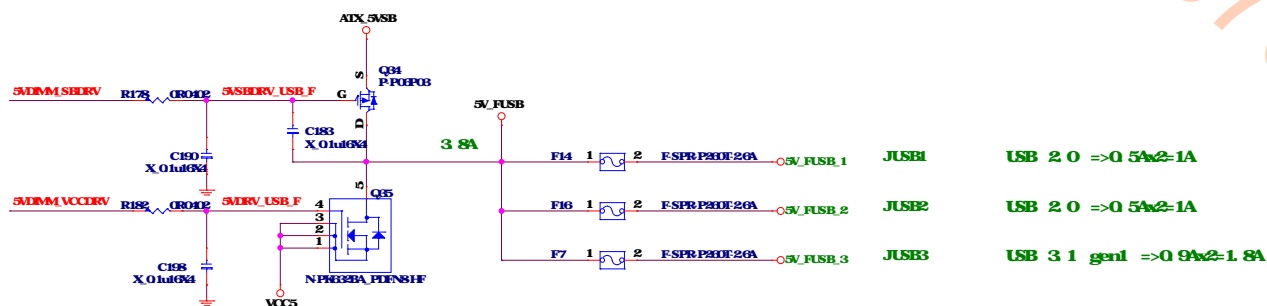
FRONT USB3.0
180



REAR USB PORT POWER



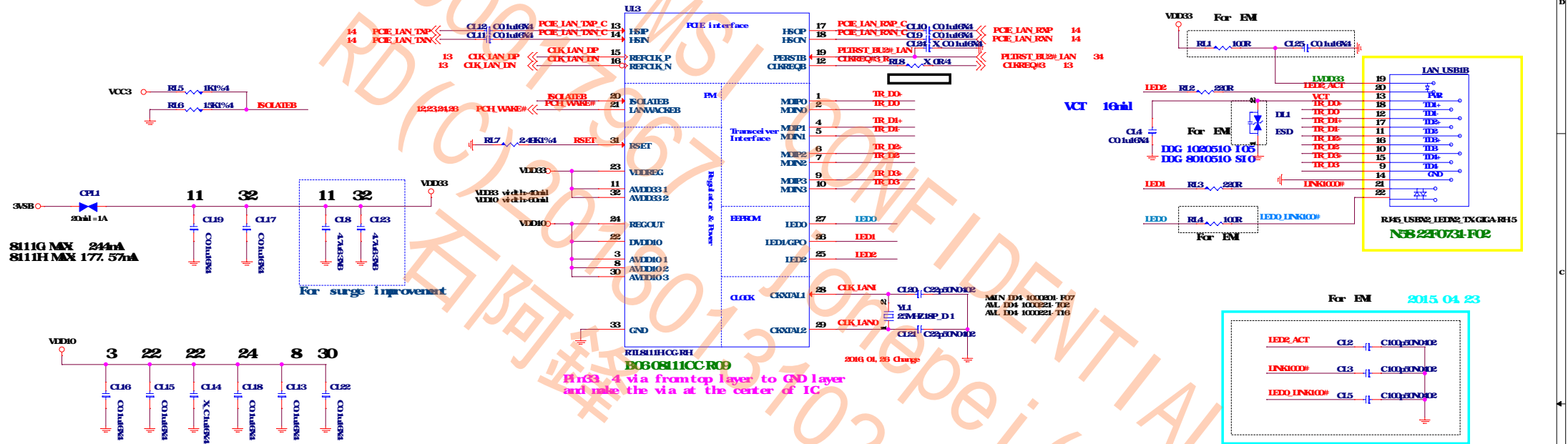
FRONT USB PORT POWER



RIL8111G/RIL8111H Giga LAN

8111H B06 08111CC R09
8111G B06 08111GC R09

LAN Connector



8111G POWER Consumption

	3.3V @ mA	mW
10 MIdle/15%	17.15/116.7	56.6/385.1
100 MIdle/15%	71.45/129.5	235.8/427.4
Giga Idle/15%	179.1/243.9	591/804.9
ALPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 MIdle/15%	9.9/84.69	32.67/279.48
100 MIdle/15%	48.11/92.44	158.76/305.05
Giga Idle/15%	124.5/177.57	410.85/585.98
ALPS	5.50	18.15

ESD Protect

U21/3 close to connector

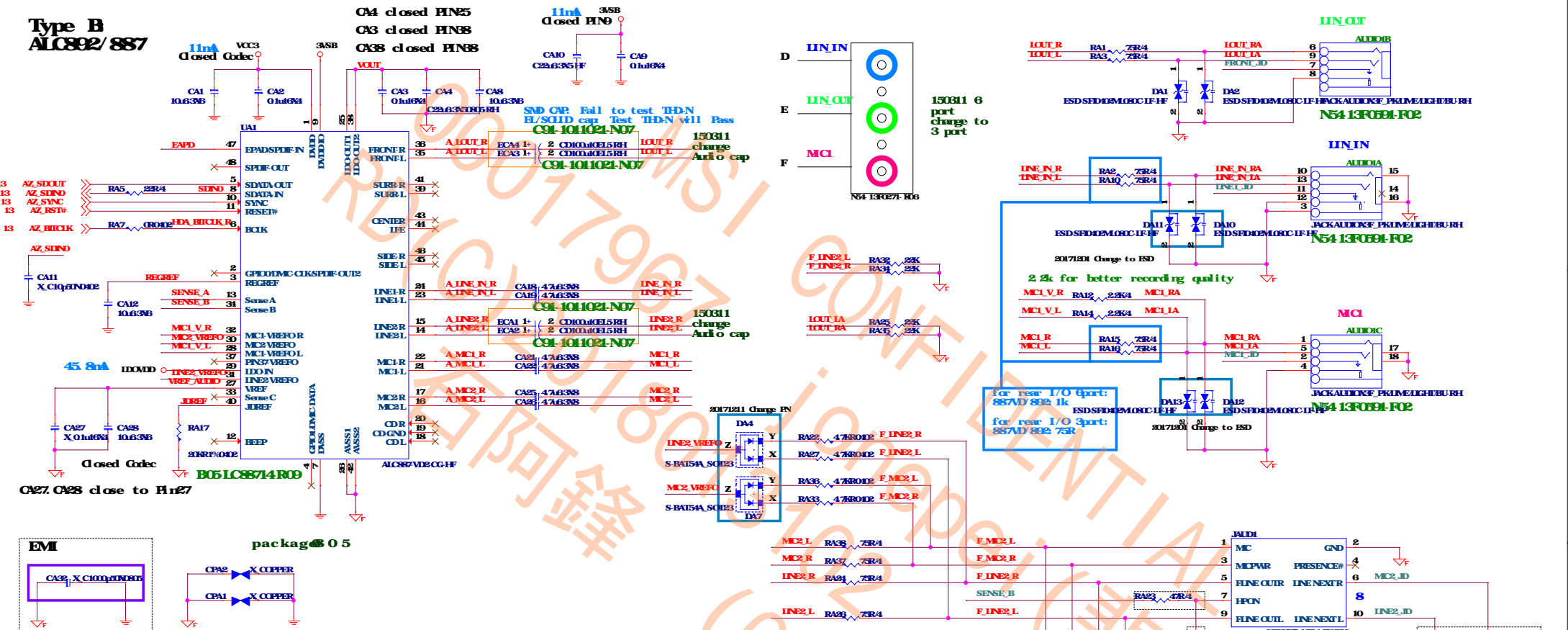


Min DOG 0200529 A66
AL: DOG 45B0510 I14

msi MICROSTAR INT'L CO., LTD.

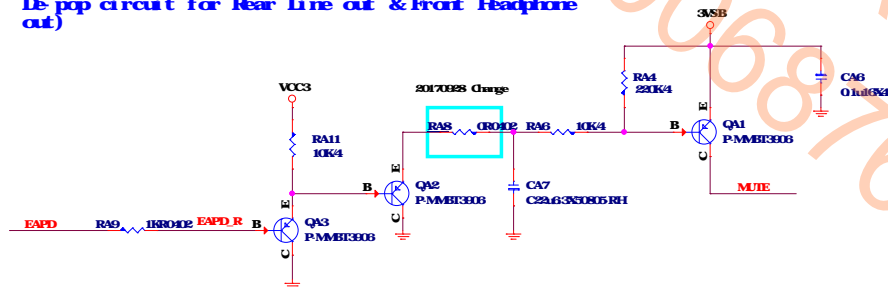
Title	LAN- RIL8111H		
Docu. Number	MS-7824		
Rev	1.00		
Date	Wednesday, January 10, 2007	Sheet	31 of 38

Type B ALC887 / 887



Rear Line OUT De-pop circuit

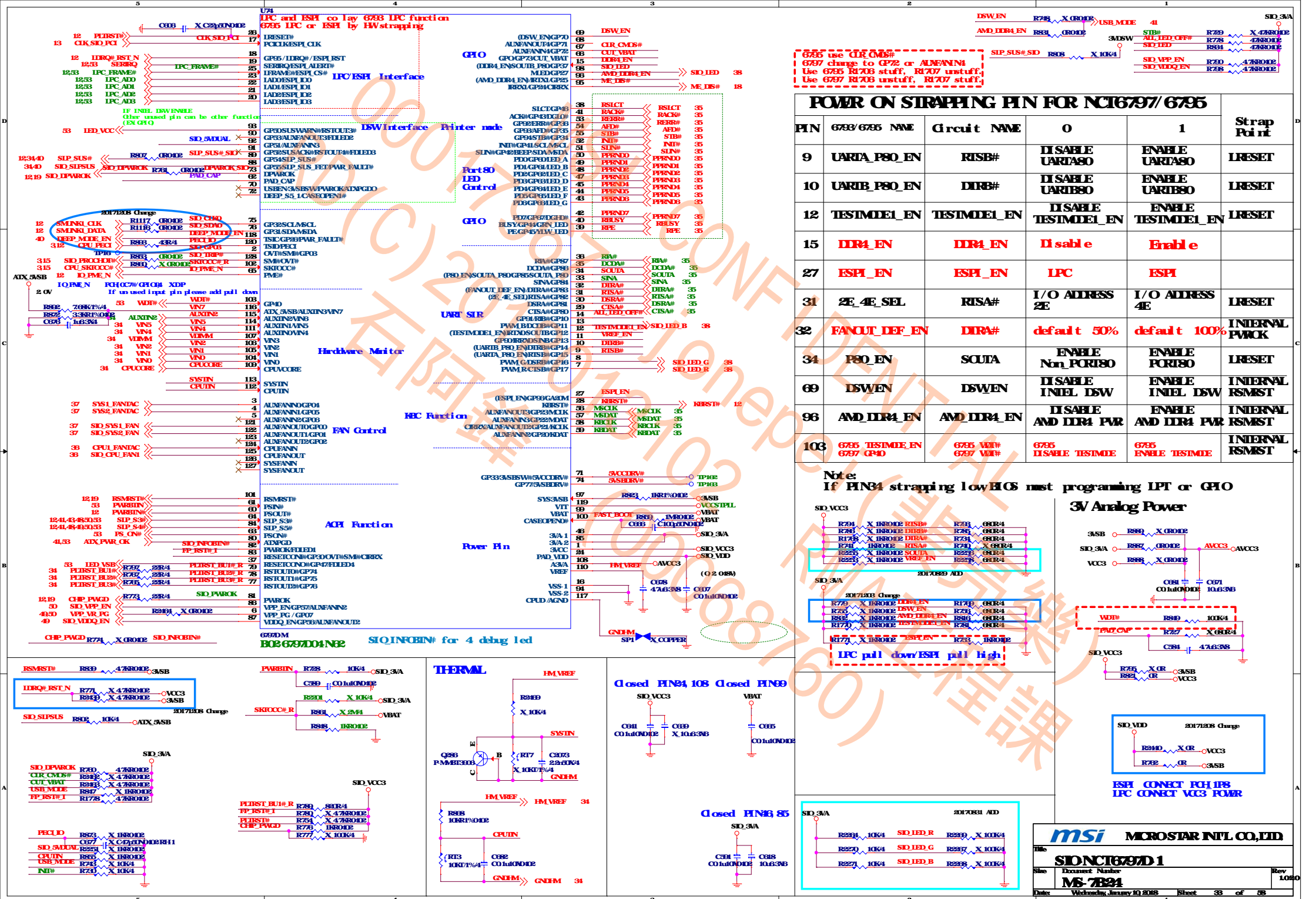
De-pop circuit for Rear Line out & Front Headphone out)

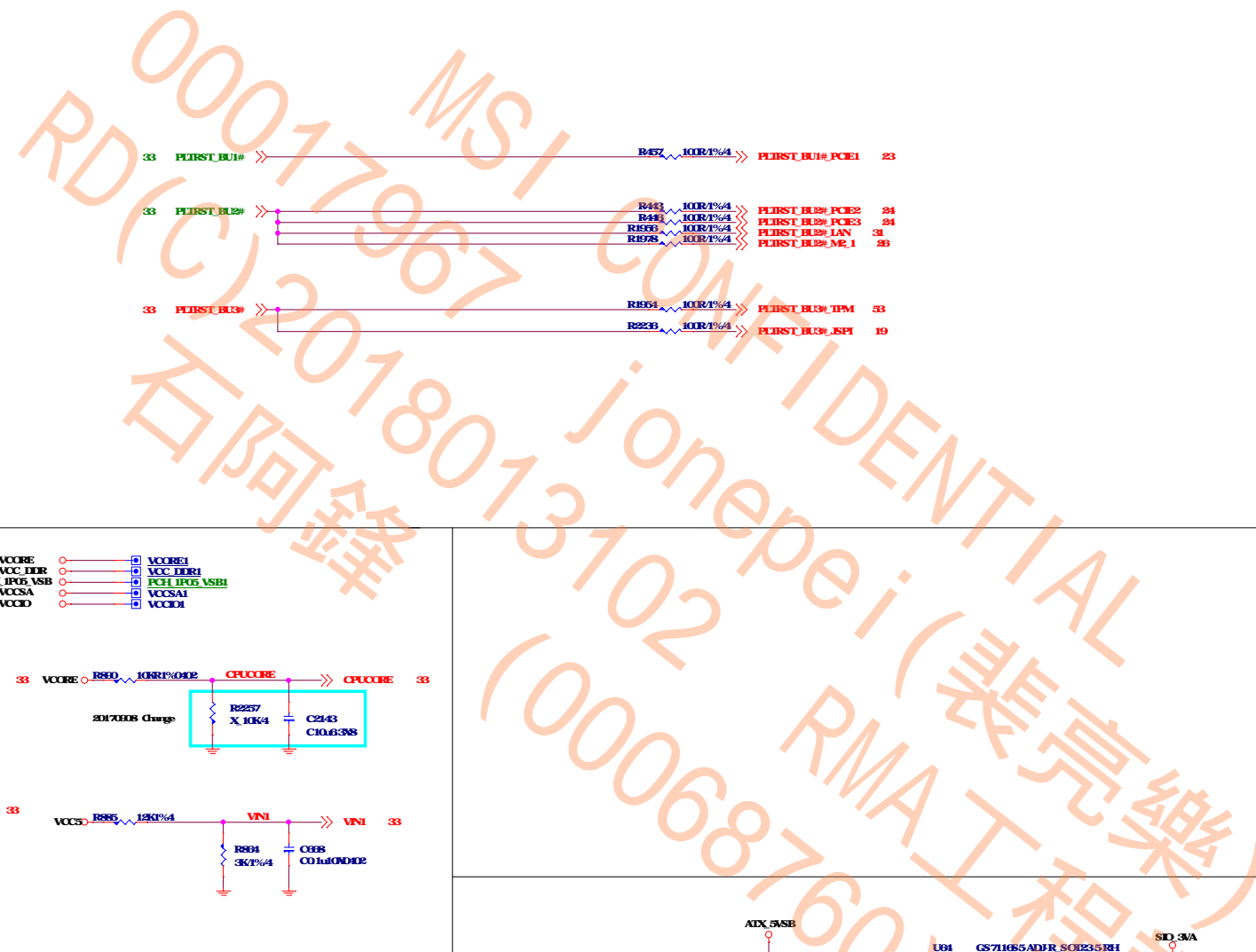


Digital

Analog

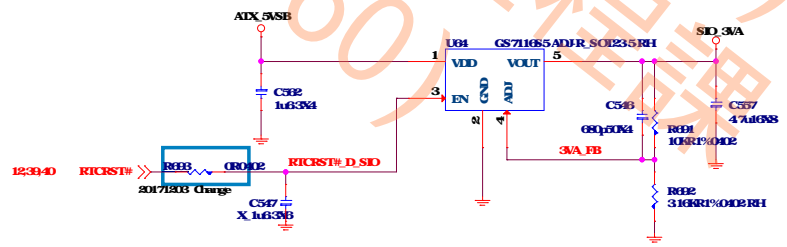
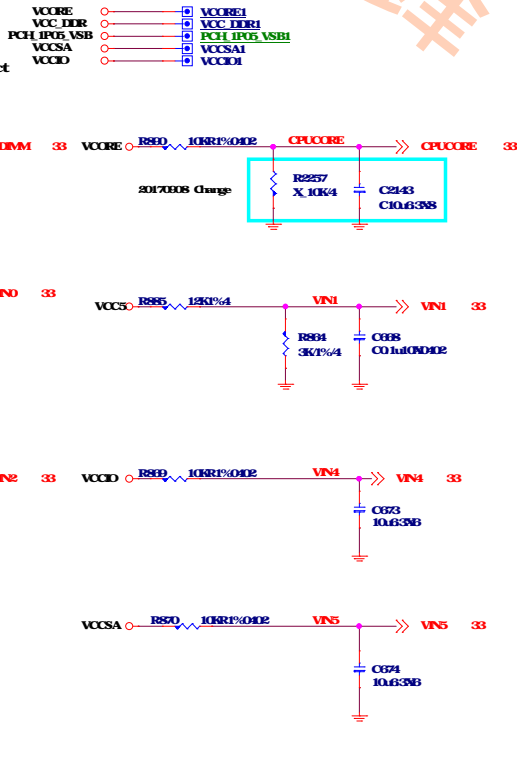







HWMonitor - Voltage

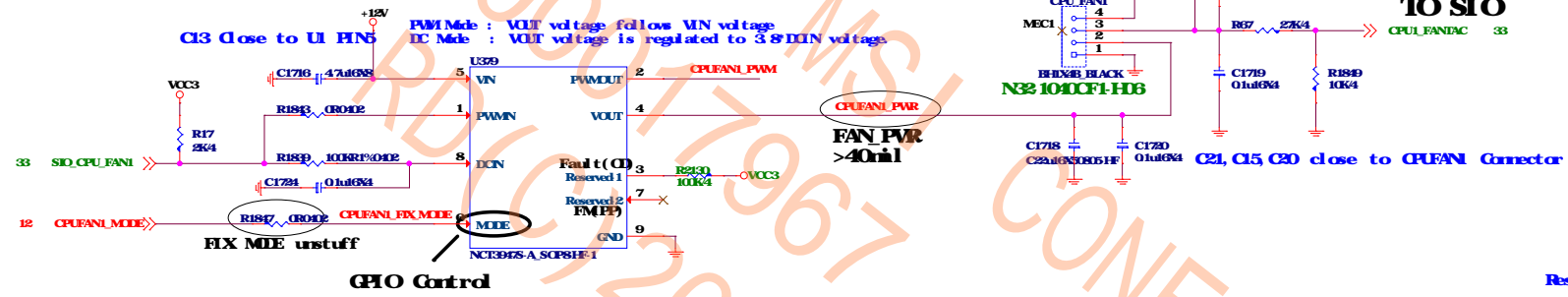
SIO HM Voltage voer 2V will not detect



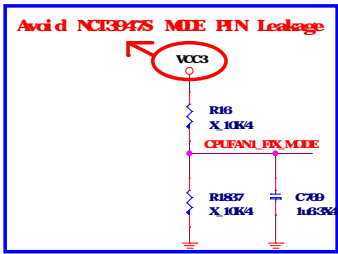
		MICROSTAR INT'L CO., LTD.	
Title			
SIDNCT679D2			
Size	Document Number	Rev	
	MS-7291	1080	
Date	Wednesday, January 10, 2006	Sheet	34 of 55

TYPE K: 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MDE

- 1. PWM/DC/OPP LED RC/B3 L D
- 2. GPIO BS PW MDC MODE
- 3. OCP GPIO BDS
- 4. PWM OR DC FAN GPIO HS
- 5. FAN S SOFTWARE GPIO

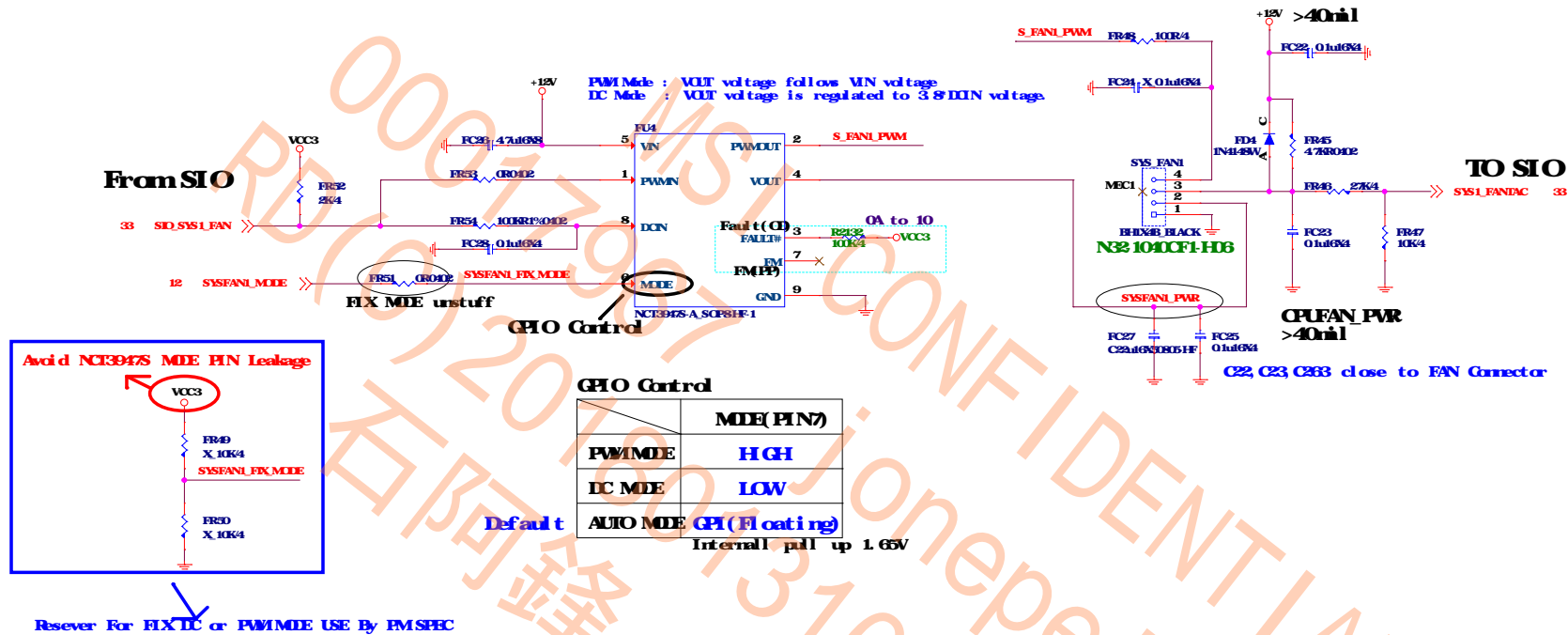


	MDE (PIN7)
PWM/DC	HIGH
DC MDE	LOW
AUTO MDE	GPIO (Floating)

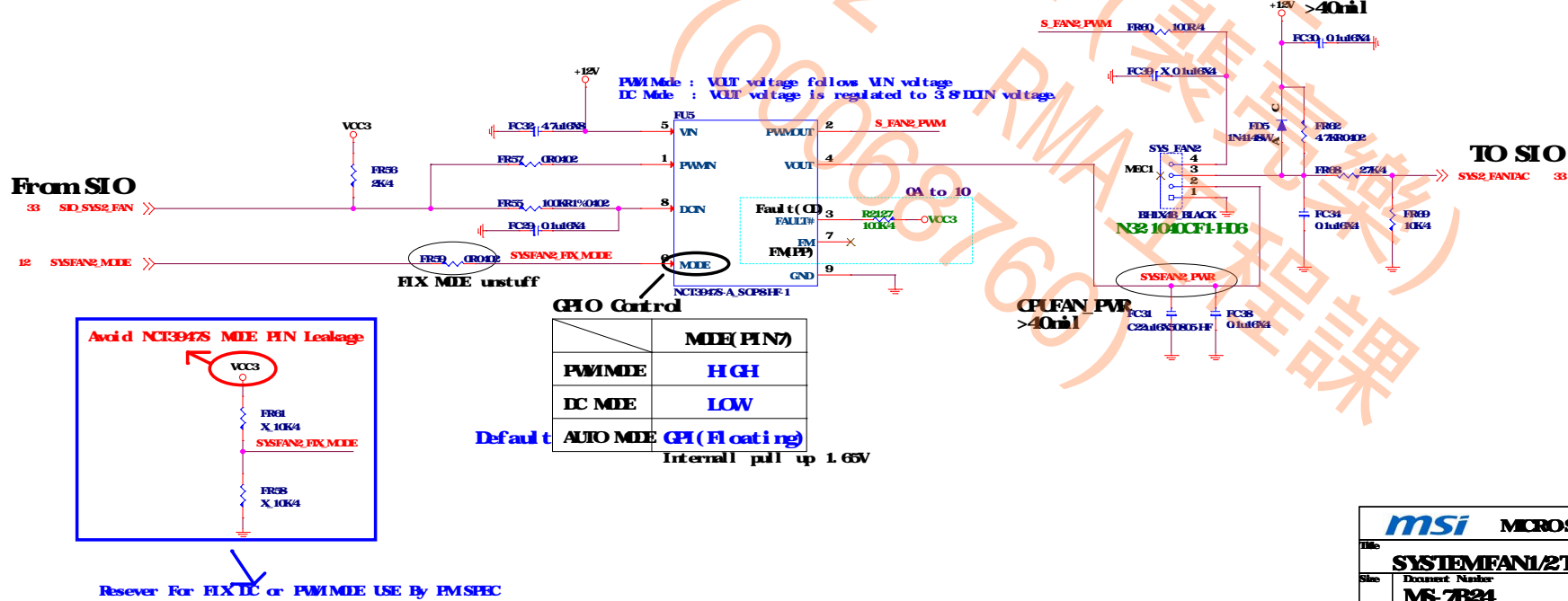


Reverse For FLY DC or PWM/DC USE By PMSPEC

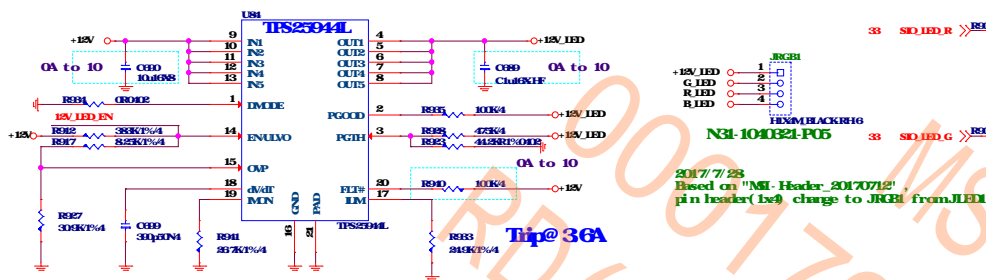
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE
2 GPIO HS PW MDC MODE



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



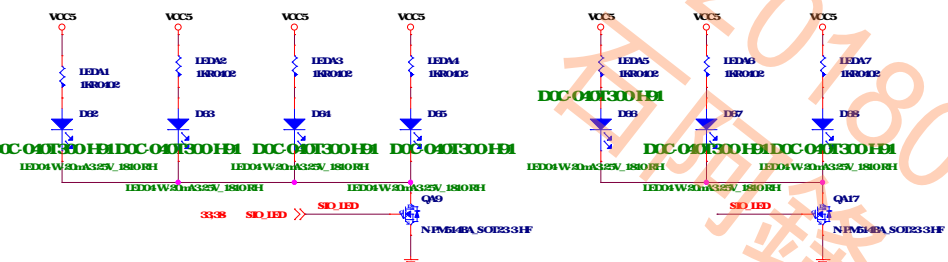
JLED



BOTTOMLED

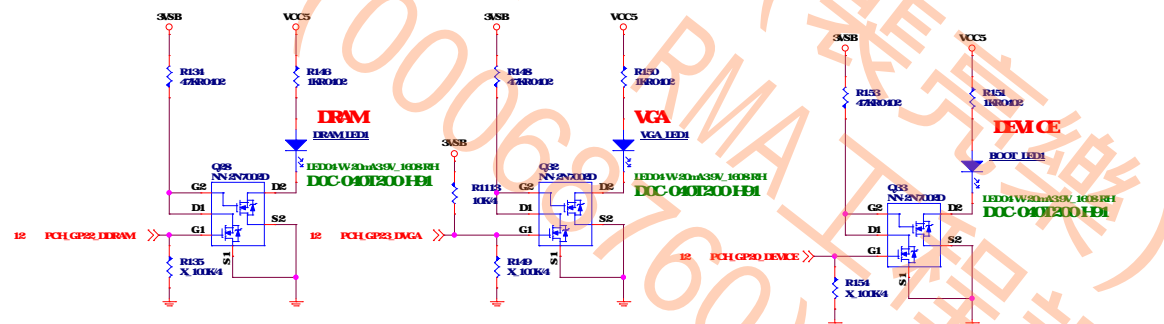
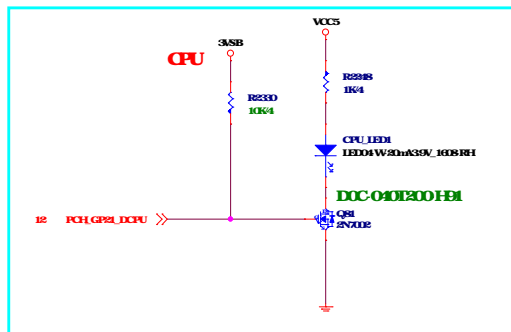
AUTOLED

Auto test is transparent and width 40mm
(): MDDC 0401300 HB1/S; DDC 0405300 E07/8



EZ DEBUG

: MDDC 0401300 HB1/ S: DDC 0405300 E07/4

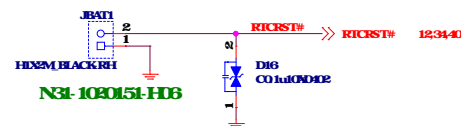
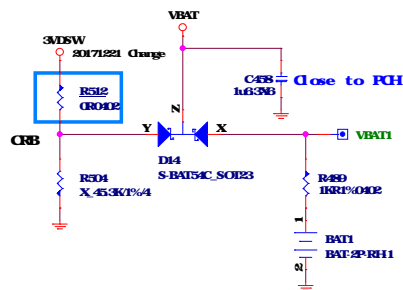
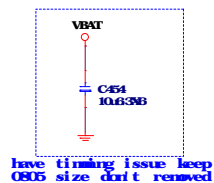


GPIO LED	PCH GP20	PCH GP21	PCH GP22	PCH GP23
	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
	NATIVE LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

- 4 LED default
1. CPU check CPU LED checkPASS
 2. Memory / memory LED checkPASS
 3. VGA check/VGA LED checkPASS
 4. LED LED

MSI CONFIDENTIAL
RD(C)2018013102
石阿鋒 jonepei (裴亮樂)
RMA工程課 (00068760)

VBAT

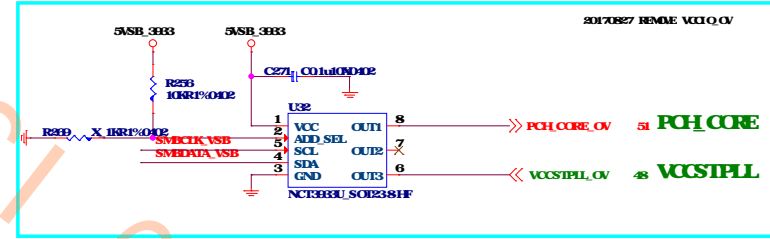
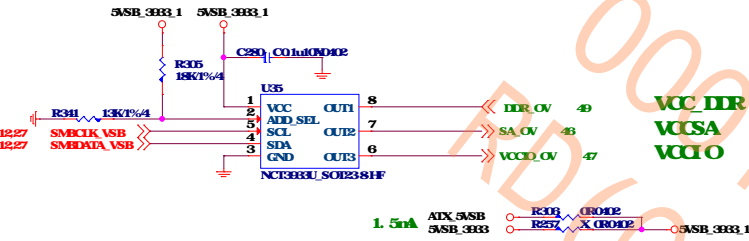


UPI VOLTAGE CONSOLE

0x20 RH=18K RL=13K

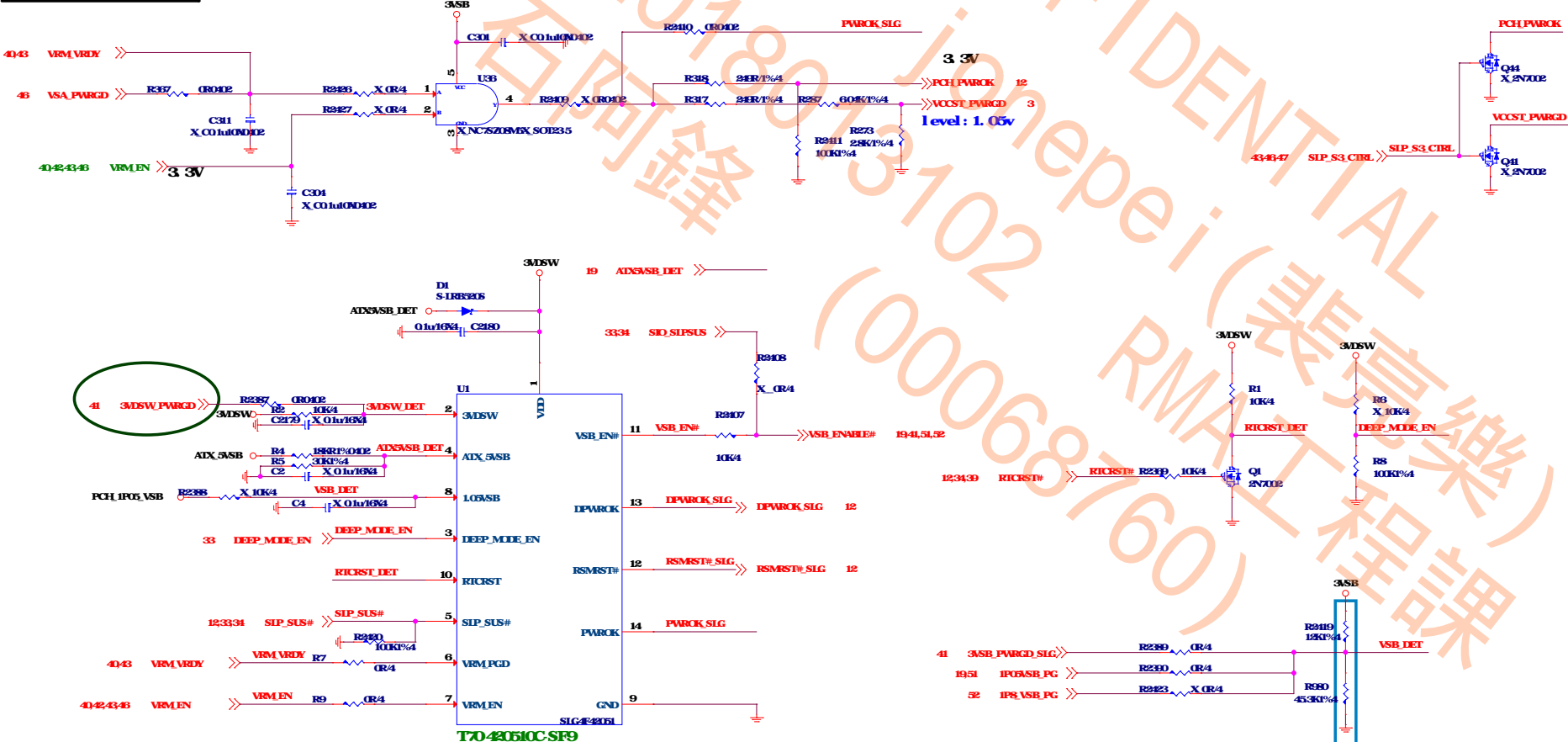
UPI VOLTAGE CONSOLE

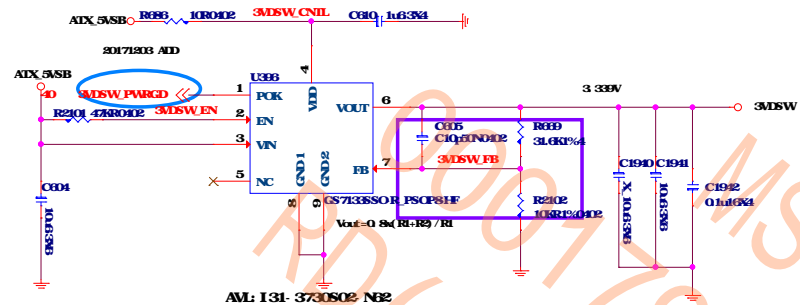
0x20 RH=10K RL=OPEN



1.5mA 5V_RUSB- R238 X OR402 5VSB_3933

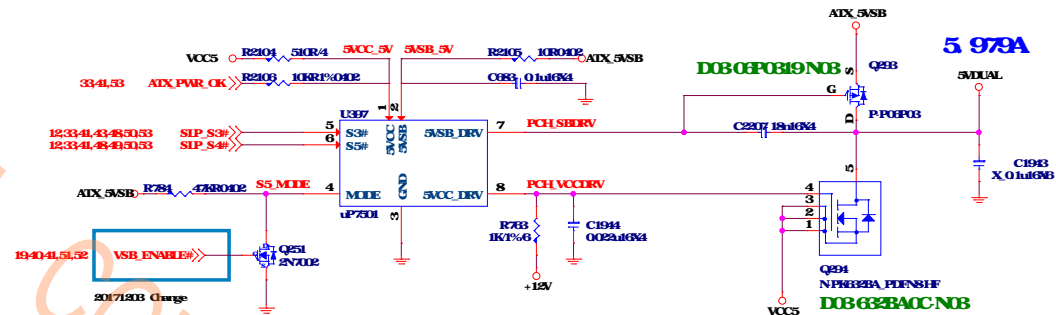
VRMSequence





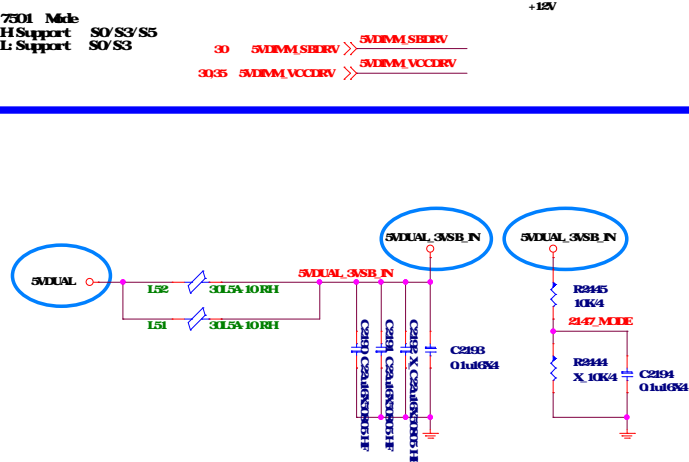
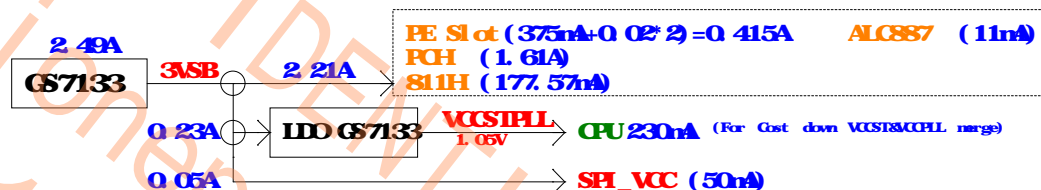
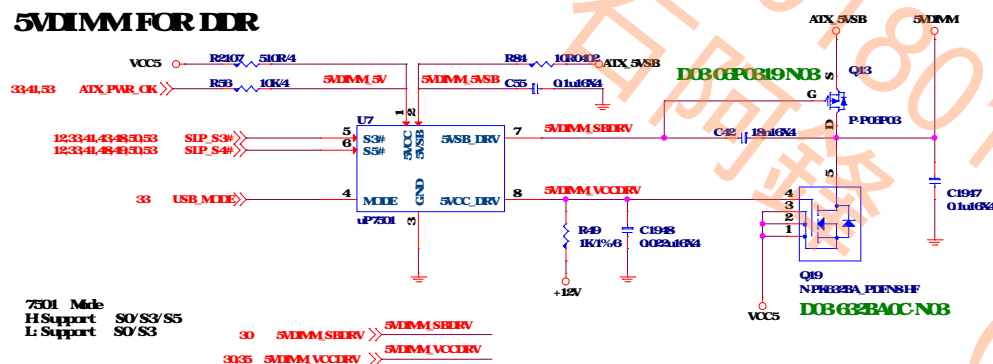
5VDUAL

5VDUAL is power source of 1F05B

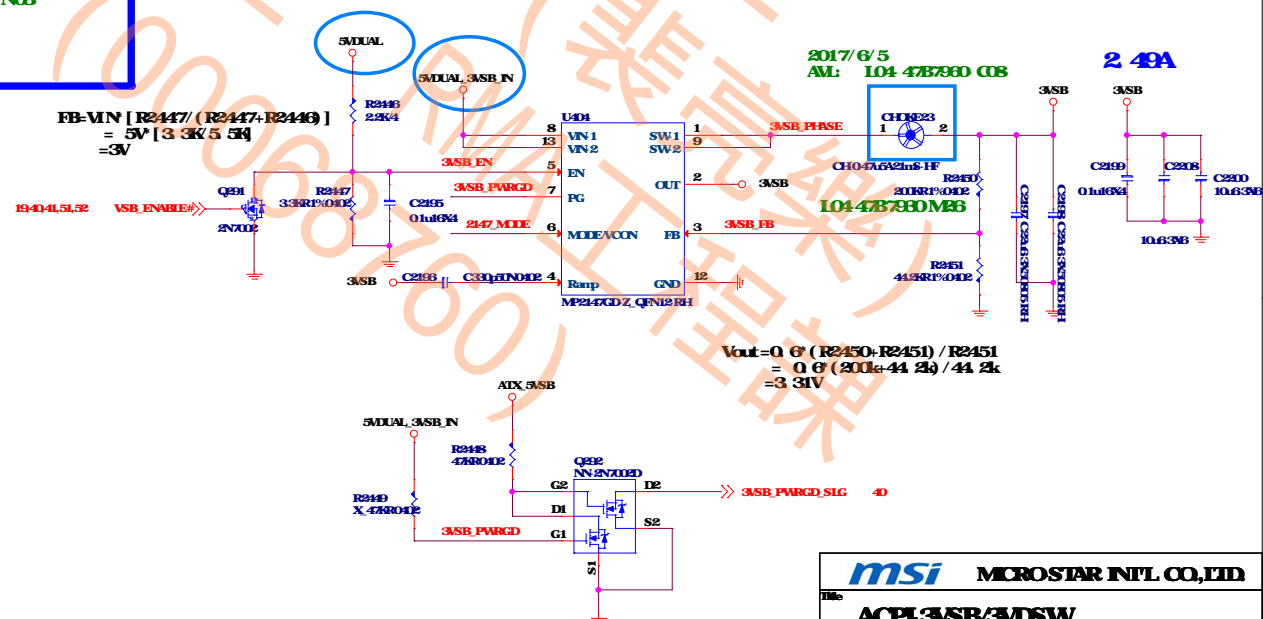


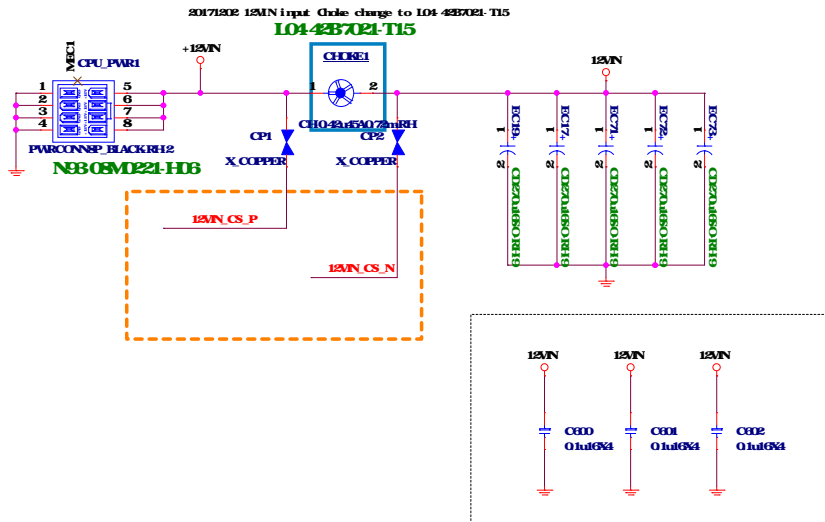
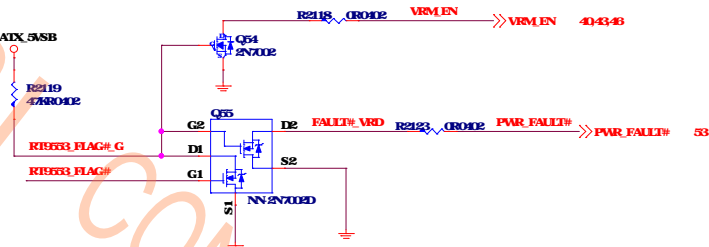
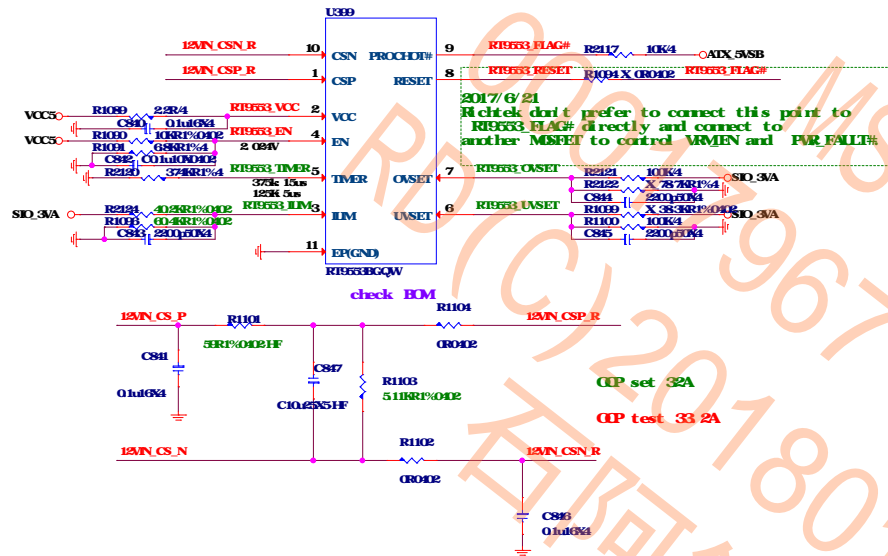
5VDIMM FOR DDR

7.022A



$$\begin{aligned} \text{FB-VIN} &= \frac{R_{2447}}{R_{2447} + R_{2446}} \cdot 5V \\ &= 5V \cdot \frac{3.3k}{5.5k} \\ &= 3V \end{aligned}$$





CORE

$$D = V_{out} / V_{in}$$

$$= 1.52 / 12$$

$$= 0.126667$$

$$N = 4$$

$$I_{rms} = I_{out} / \sqrt{N \cdot SQR(ND \cdot (1 - ND))}$$

$$= 138 / \sqrt{4 \cdot SQR(4 \cdot 0.126667 \cdot (1 - 4 \cdot 0.126667))}$$

$$= 17.249A$$

GE

$$D = V_{out} / V_{in}$$

$$= 1.52 / 12$$

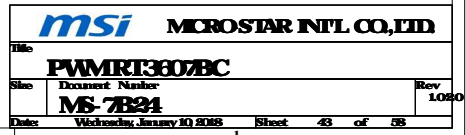
$$= 0.126667$$

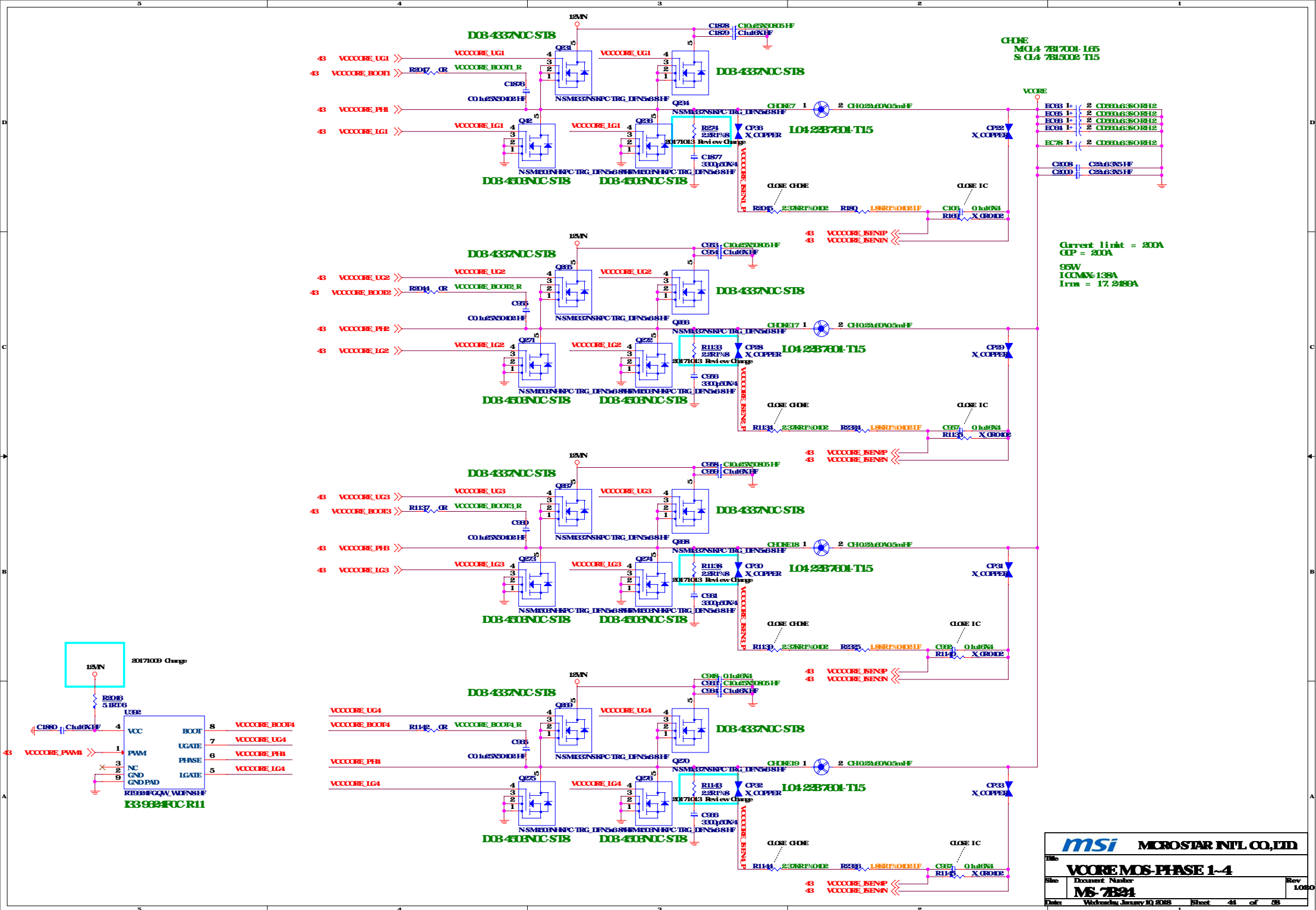
$$N = 2$$

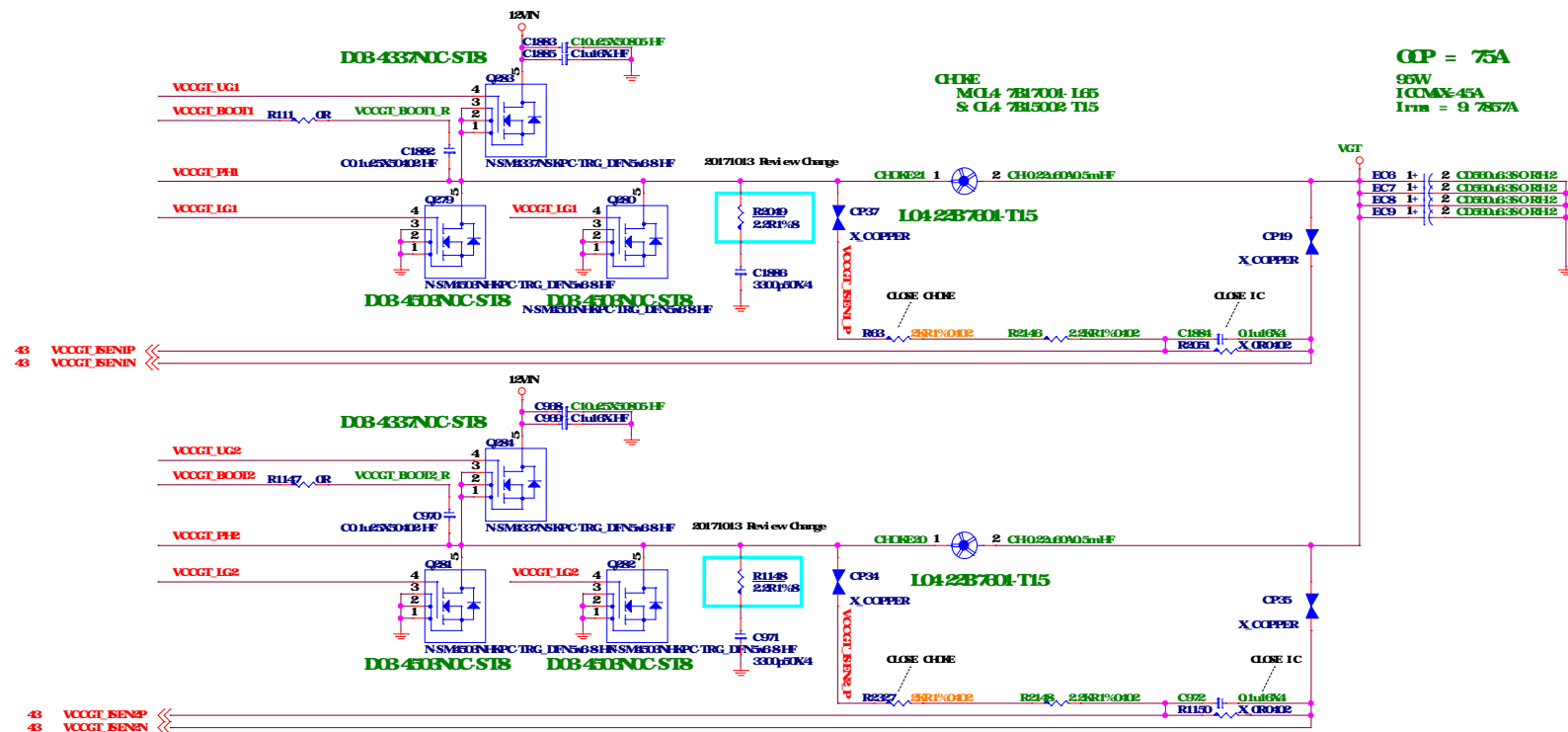
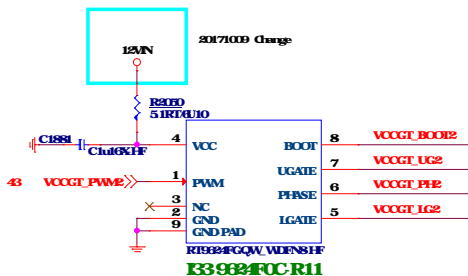
$$I_{rms} = I_{out} / \sqrt{N \cdot SQR(ND \cdot (1 - ND))}$$

$$= 45 / \sqrt{2 \cdot SQR(2 \cdot 0.126667 \cdot (1 - 2 \cdot 0.126667))}$$

$$= 9.7857A$$







SA Power: 1.05V, 123A

Rocpset: 5.6K
 OCP(min) = Rocpset * Iocset / Rison (Low side)
 = 5.1K * 10uA / 3.3mhm
 = 15.45A

OCP(max) = Rocpset * Iocset / Rison (Low side)
 = 5.1K * 10uA / 2.1mhm
 = 24.2A

OCP(test) = 19.2A

Rison (Low 10V)
 DB 632BAC N03 :
 Max 3.3mhm Type 2.1mhm

up1540 C5/R115 no stuff

2014.12.25
 for up1540 C39 is OCP set min 5K ohm
 stuff 5.3K OCP SEE 15.76A

2014.08.25 update

K38125E0CR11

$$V_{out} = V_{ref} * (R2057 + R2058) / R2058$$

$$= 0.8 * (1k + 3.16k) / 3.16k$$

$$= 1.053V$$

$$I_{rms} = I_{out} * \sqrt{R_{DS(on)} * (V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 18 * 0.2825$$

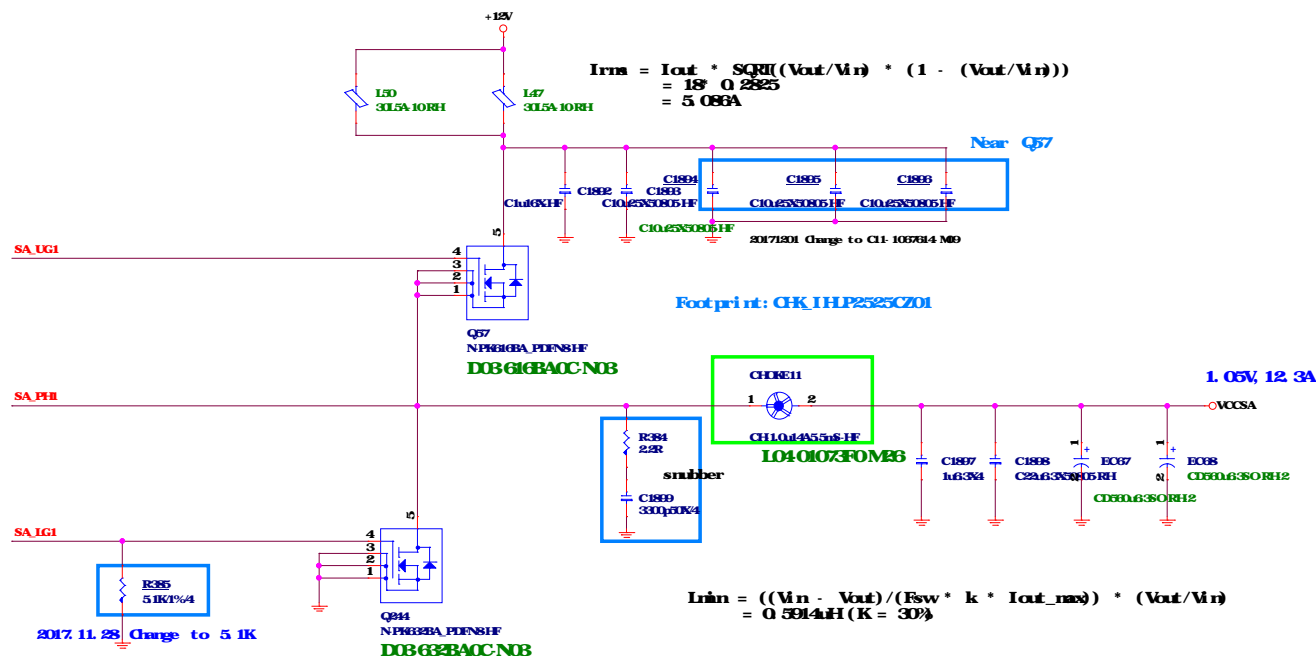
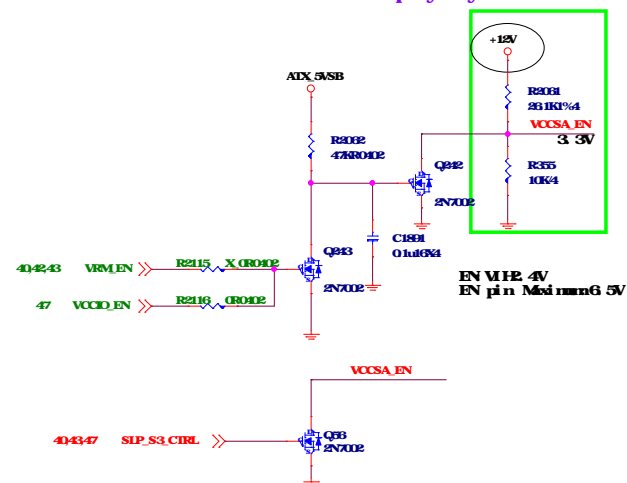
$$= 5.086A$$

Footprint: CH11HP2525C201

$$I_{lim} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

$$= 0.5914uH (K = 30\%)$$

R11 up by layout & Check Level

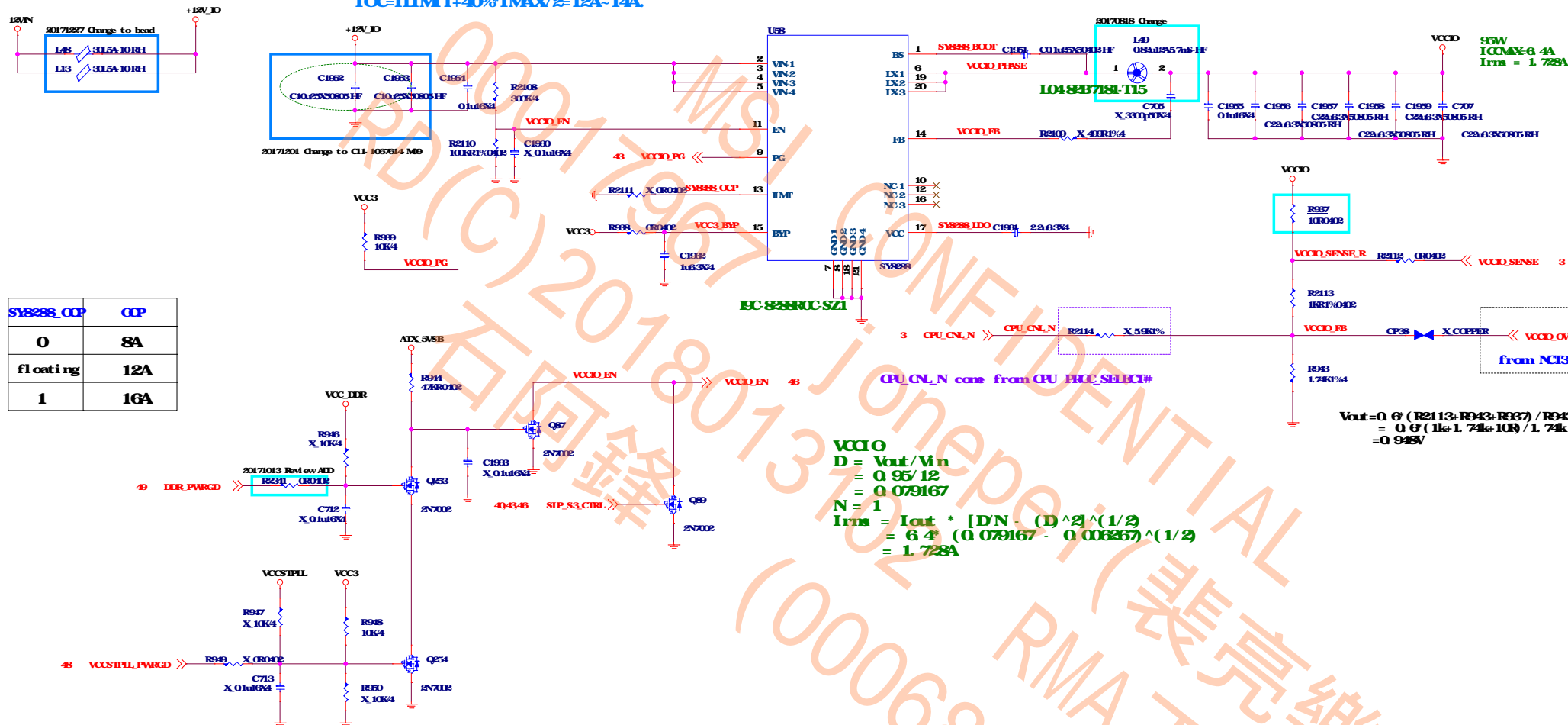


SLP_S3# assertion to VCC, VCCGE, VCCIO and VCCSA rails completely off.

SLP_S3# assertion to VR disabled max 1us

IO Power: 0.95V, 64A

IMAX 10A
ILIMT=10A~12A
IOC=ILIMT+40%*IMAX/2=12A~14A.



SY8288_OOP	OOP
0	8A
floating	12A
1	16A

```

VccIO
D = Vout/Vin
  = 0.95/12
  = 0.079167
N = 1
Irms = Iout * [D*N - (D^2)^(1/2)
  = 6.4 * (0.079167 - 0.00625)^(1/2)
  = 1.728A

```

$$\begin{aligned} V_{out} &= 0.6 \text{ V} \cdot (R_{2113} + R_{943} + R_{937}) / R_{943} \\ &= 0.6 \text{ V} \cdot (1\text{k} + 1.74\text{k} + 10\text{k}) / 1.74\text{k} \\ &= 0.945\text{V} \end{aligned}$$

For Cost down VCST&CCPL merge



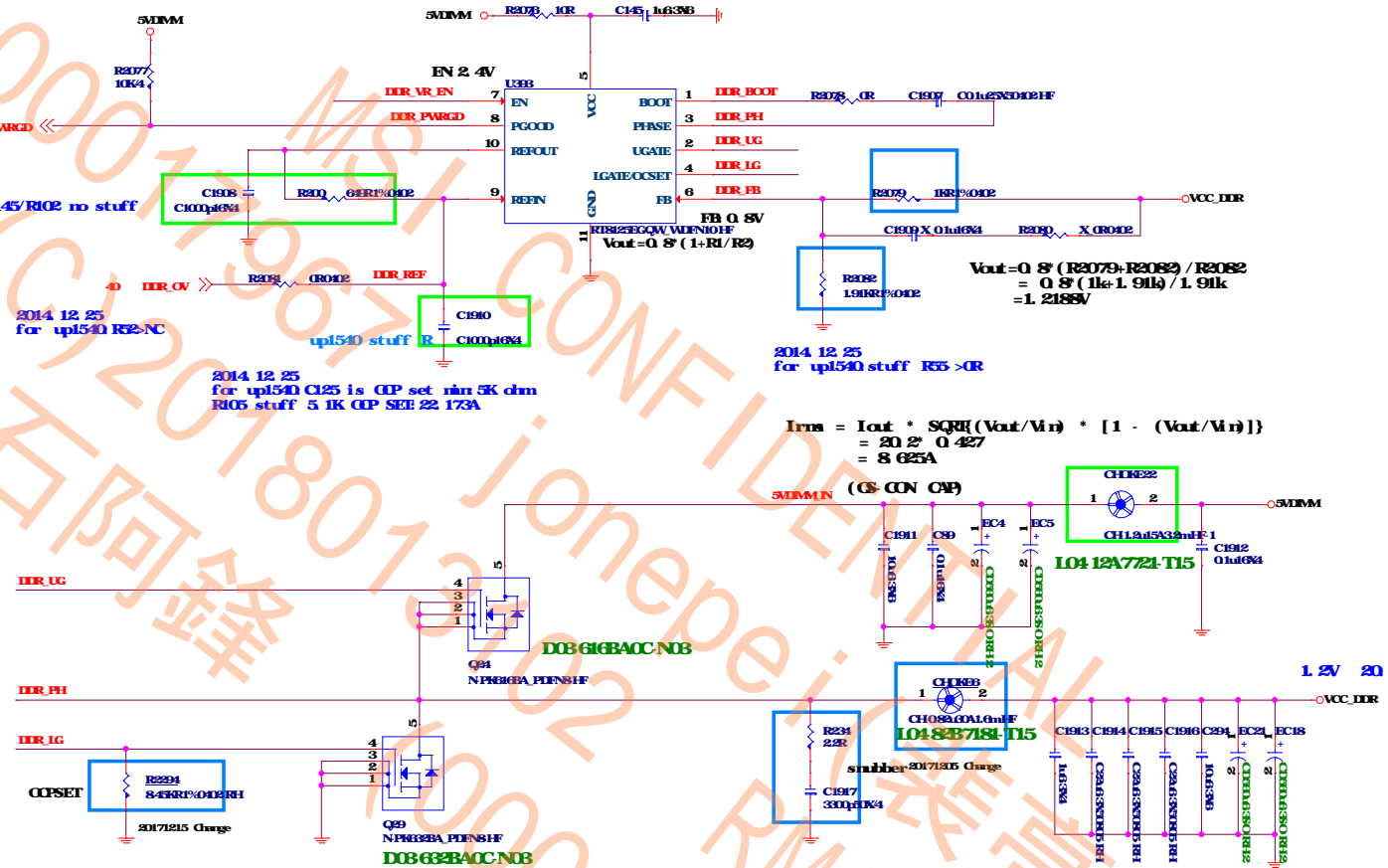
1.2A FOR DDR VTT

Rocpset: 6 04K

$$\begin{aligned} OCP(\text{type}) &= R_{ocset} * I_{ocset} / R_{lson}(\text{Low side}) \\ &= 8.45k * 10mA / 4.6m\Omega \\ &= 18.3A \end{aligned}$$
$$\begin{aligned} I_{OP(max)} &= R_{ocset} * I_{ocset} / R_{lson}(Low \text{ side}) \\ &= 8.45K * 10uA / 3m\Omega \\ &= 28.2A \end{aligned}$$

OOP(test) = 23.4A

Rdson(low) 4.5V
IDB 632BA0G NOB :
MAX 4.6uAhm TYPE 3uAhm

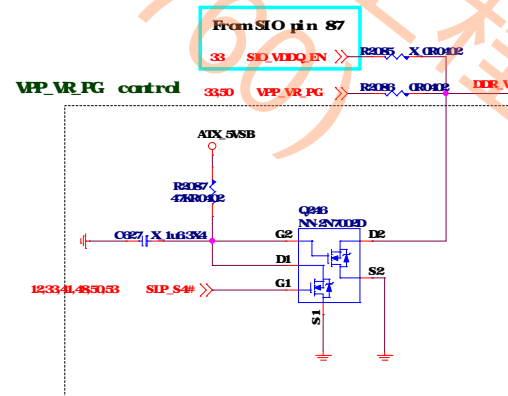


Dat as heet

$$I_{in} = ((V_{in} - 1.2V) / (F_{sw} * k * I_{out_max})) * (V_{out} / V_{in})$$

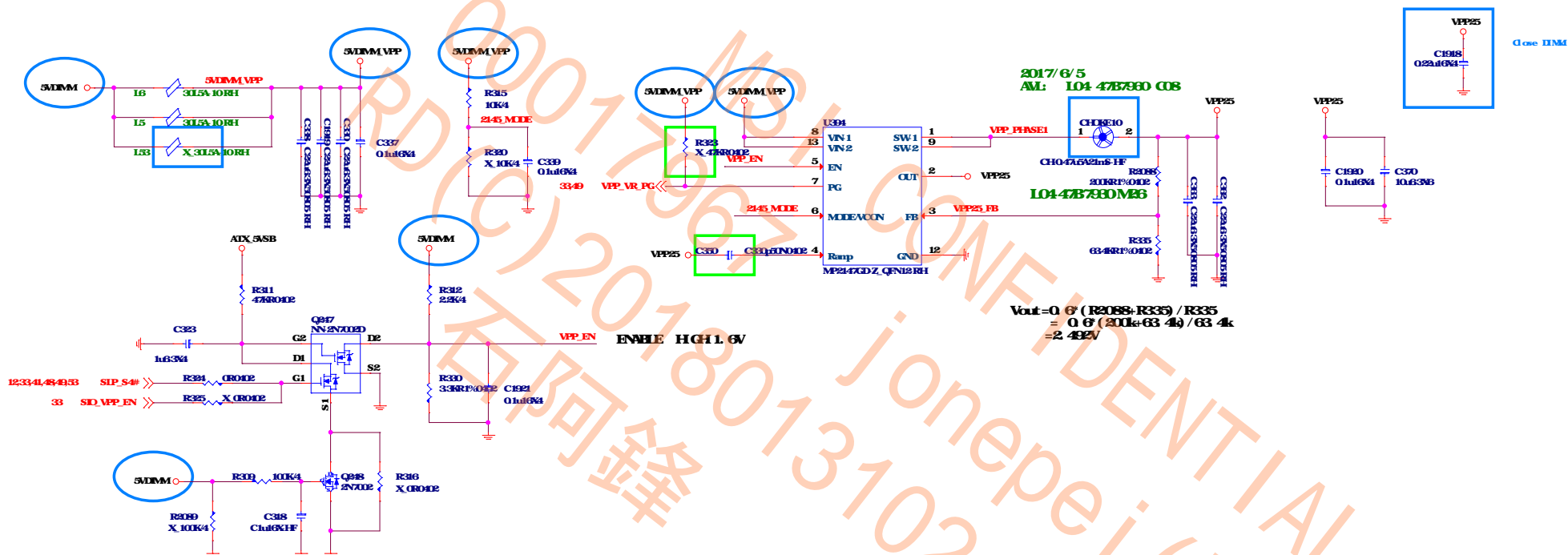
$$= 0.7677 \mu H \text{ (K = 30\%)}$$

C A P R , 0 2 3 9 H L 1. 2 8 9 W H



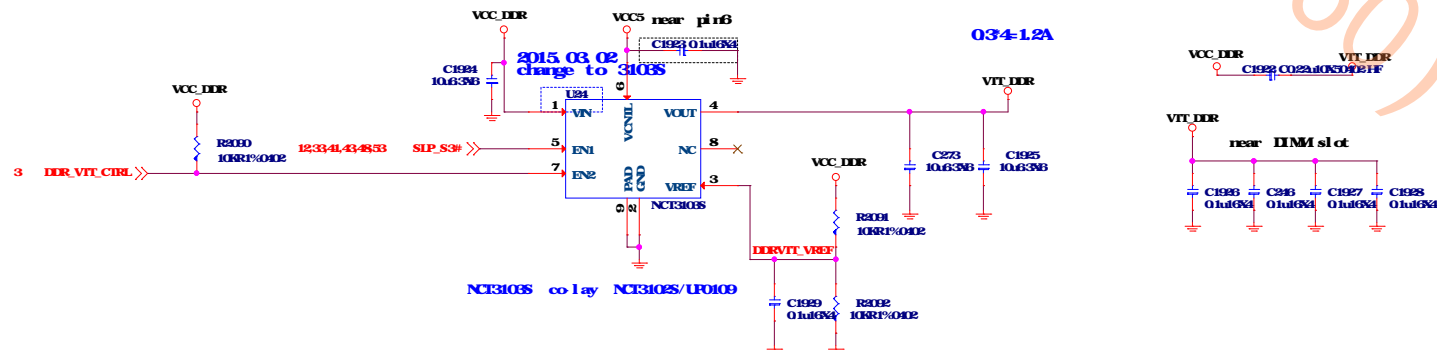
4DIMM:2 24A FOR DDR VPP2.5V


VPP25 Power
2 5V; 2 24A



To make sure VPP EN after 5MINM stable

DDR VTT Power



 MICROSTAR INT'L CO., LTD.			
Title DDR PWR VPP25 MP2147/VT			
Size	Document Number MS-7B24		Rev 1.02B
Date	Wednesday, January 30 2008	Sheet	30 of 56

PCH 1VSB

1.05V 11.576A

Rocpset: 6.04K
 $OCF(type) = Rocpset * 10uA / Rlsor(LOW side)$
 $= 5.6K * 10uA / 4.6uA$
 $= 12.1A$
 $OCF(max) = Rocpset * 10uA / Rlsor(LOW side)$
 $= 5.6K * 10uA / 3uA$
 $= 18.6A$

OCF(test) = 17.16A

Rlsor(LOW) 4.5V
 DB 632BAOC N03 :
 MX 4.6uA TYPE 3uA

$$I_{rms} = I_{out} * \sqrt{SQRT(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 10.68A * 0.4$$

$$= 4.265A < 5000mA$$

L04 47B730 T15 for OC Gating 10 9 7 5
 L04 12A7321-165 for Gating 3 SLI, ECO
 L04 12A721-115 for cost down

$I_{in} = 13.11A * 1.05V / 0.8 / 5V = 3.44A$
 L02 3008043 M26

MX 11.576A

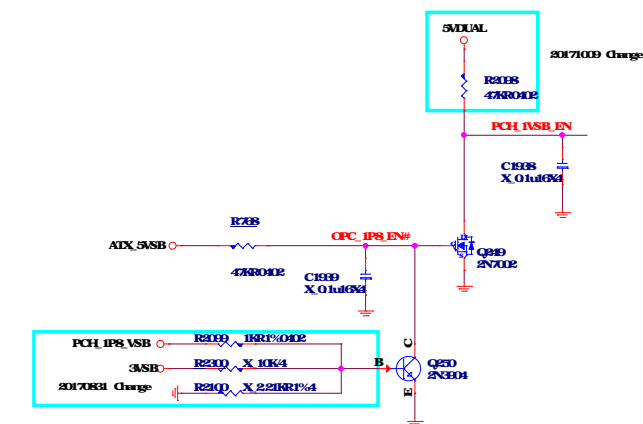
$$I_{lim} = ((V_{in} - V_{out}) / (f_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

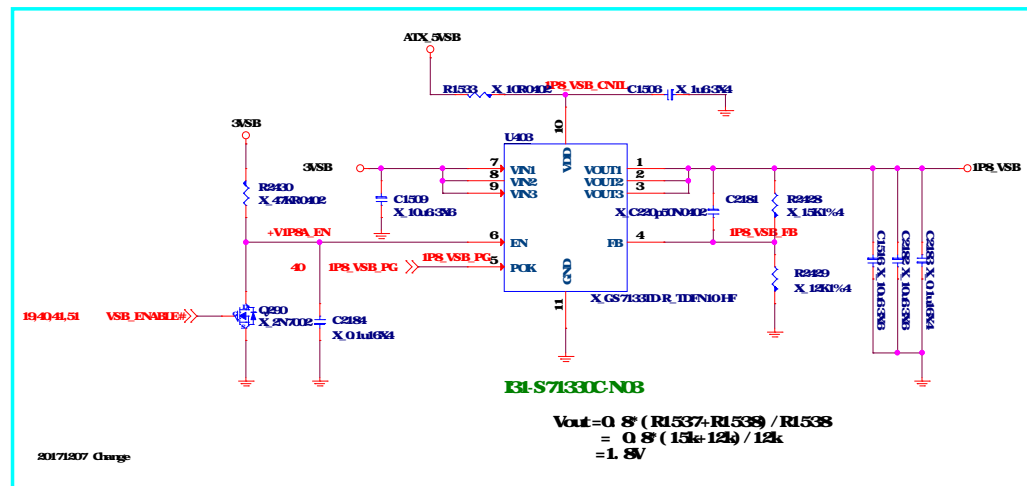
$$= 0.833uH (K = 30\%)$$

$$V_{out} = V_{ref} * (((R2097 - R750) / R750))$$

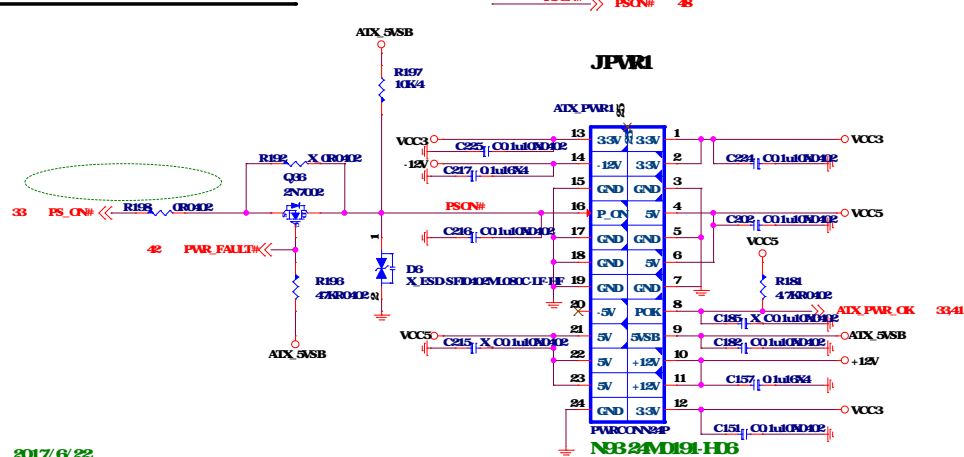
$$= 0.8 * (((3.16K - 1K) / 3.16K))$$

$$= 1.053V$$



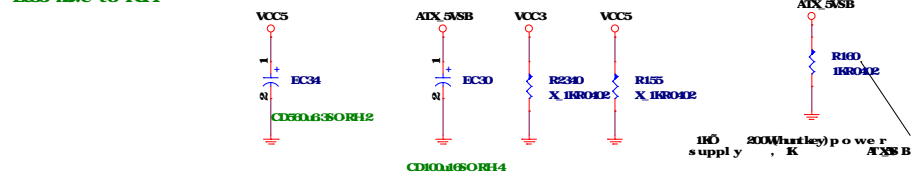


ATX POWER CONNECTOR

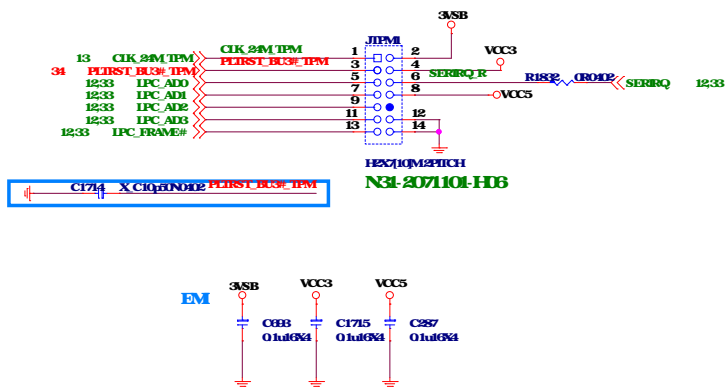


2017/6/22
EC34, EC36 are changed from 470uF to 560uF by buyer request

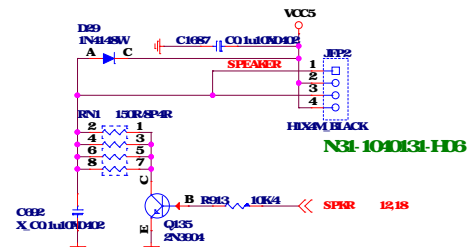
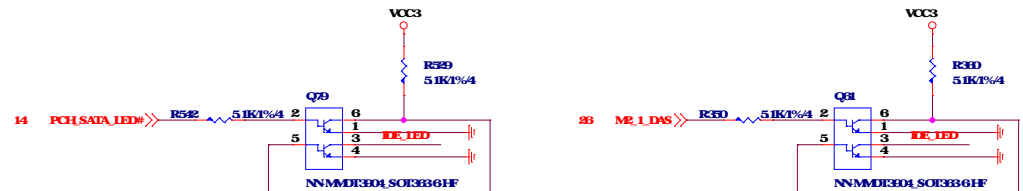
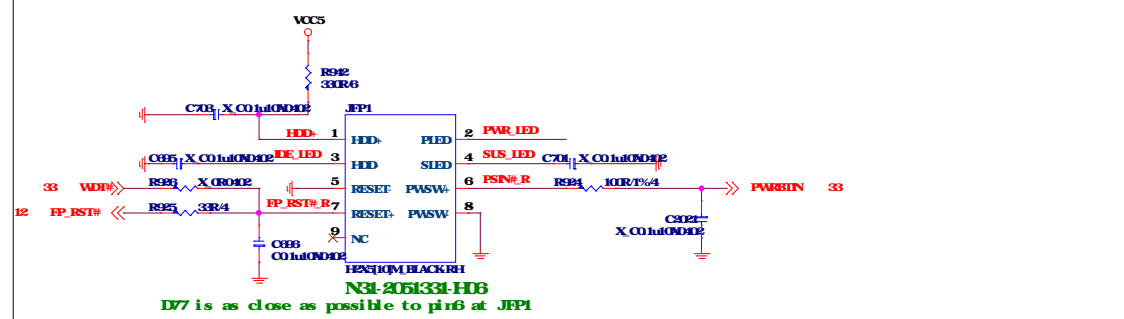
2017/ 7/ 6
EC36 move to PCI 1



TPMPi n Header



FRONT PANNEL



Front Panel LED

